NELLCOR

SERVICE MANUAL

NPB-4000/4000C
Patient Monitor

MALLINCKRODT

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CE 0123

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Mallinckrodt Inc.
675 McDonnell Boulevard
P.O. Box 5980
St. Louis, MO 63134
Telephone 314.654.2000
Toll Free 1.800.635.5267

Mallinckrodt
Europe BV
Hambakenwettering 1
5231 DD's-Hertogenbosch
The Netherlands
Telephone +31.73.6485200

Nellcor Puritan Bennett Inc.
4280 Hacienda Drive
Pleasanton, CA 94588

To obtain information about a warranty, if any, for this product, contact Mallinckrodt Technical Services or your local Mallinckrodt representative.

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SECTION 1: INTRODUCTION

1.1 Manual Overview
1.2 Warnings, Cautions, and Notes
1.3 NPB-4000/C Patient Monitor Description
1.4 Related Documents

1. INTRODUCTION

1.1 MANUAL OVERVIEW

This manual contains information for servicing the model NPB-4000 and NPB-4000C patient monitor, subsequently referred to as NPB-4000/C throughout this manual. Only qualified service personnel should service this product. Before servicing the NPB-4000/C, read the operator's manual carefully for a thorough understanding of operation.

1.2 WARNINGS, CAUTIONS, AND NOTES

This manual uses three terms that are important for proper operation of the monitor: Warning, Caution, and Note.

1.2.1 Warning

A warning precedes an action that may result in injury or death to the patient or user. Warnings are boxed and highlighted in boldface type.

1.2.2 Caution

A caution precedes an action that may result in damage to, or malfunction of, the monitor. Cautions are highlighted in boldface type.

1.2.3 Note

A note gives information that requires special attention.

1.3 NPB-4000/C PATIENT MONITOR DESCRIPTION

The purpose and function of the NPB-4000/C patient monitor is to monitor: ECG; heart rate; noninvasive blood pressure (systolic, diastolic, and mean arterial pressures); functional arterial oxygen saturation; respiration rate; and temperature for adult and pediatric patients in all hospital areas and hospital-type facilities. It may be used during hospital transport and in mobile, land-based environments, such as ambulances.

The physical and operational characteristics of the monitor are described in the operator's manual and in the **Specifications** section of this manual.

1.4 RELATED DOCUMENTS

To perform test and troubleshooting procedures and to understand the principles of operation and circuit analysis sections of this manual, you must know how to operate the monitor. Refer to the NPB-4000/C operator's manual. To understand the various Nellcor sensors, ECG leads, blood pressure cuffs, and temperature probes that work with the monitor, refer to the individual directions for use that accompany these accessories.

SECTION 2: ROUTINE MAINTENANCE

2.1 Cleaning
2.2 Periodic Safety and Functional Checks
2.3 Batteries
2.4 Environmental Protection

2. ROUTINE MAINTENANCE

2.1 CLEANING

WARNING: Do not immerse the NPB-4000/C or its accessories in liquid or clean with caustic or abrasive cleaners. Do not spray or pour any liquid on the monitor or its accessories.

To clean the NPB-4000/C, dampen a cloth with a commercial, nonabrasive cleaner and wipe the exterior surfaces lightly. Do not allow any liquids to come in contact with the power connector or switches. Do not allow any liquids to penetrate connectors or openings in the instrument. For cables, sensors and cuffs, follow the cleaning instructions in the directions for use that accompany these accessories.

2.2 PERIODIC SAFETY AND FUNCTIONAL CHECKS

The NPB-4000/C requires no routine service or calibration other than cleaning and battery maintenance. The following performance verification tests may be used following repair or during routine maintenance (if required by your local institution).

1. Inspect the exterior of the NPB-4000/C for damage.

2. Inspect labels for legibility. If the labels are not legible, contact Mallinckrodt Technical Services Department or your local Mallinckrodt representative.

3. Verify that the unit performs properly as described in paragraph 3.3.

4. Perform the electrical safety tests detailed in paragraph 3.4. If the unit fails these electrical safety tests, do not attempt to repair. Contact Mallinckrodt Technical Services Department or your local Mallinckrodt representative.

2.3 BATTERIES

If the NPB-4000/C has not been used for a long period of time, the battery will need charging. To charge the battery, connect the NPB-4000/C to an AC outlet or external DC supply as described in Paragraph 3.3.1 in this service manual or the **Setup and Use** section of the operator's manual.

Note: Storing the NBP-4000/C for a long period without charging the battery may degrade the battery capacity. A complete battery recharge requires 8 hours. The battery may require a full charge/discharge cycle to restore normal capacity.

Mallinckrodt recommends that the NPB-4000/C's sealed, lead-acid batteries be replaced at 2-year intervals. Refer to Section 6, *Disassembly Guide.*

2.4 ENVIRONMENTAL PROTECTION

Follow local governing ordinances and recycling plans regarding disposal or recycling batteries and other device components.

SECTION 3: PERFORMANCE VERIFICATION

3.1 Introduction
3.2 Equipment Needed
3.3 Performance Tests
3.4 Safety Tests

3. PERFORMANCE VERIFICATION

3.1 INTRODUCTION

This section discusses the tests used to verify performance following repairs or during routine maintenance. All tests can be performed without removing the NPB-4000/C covers.

If the NPB-4000/C fails to perform as specified in any test, repairs must correct the problem before the monitor is returned to the user.

3.2 EQUIPMENT NEEDED

Table 3-1 lists the equipment required for performance verification.

Table 3-1: Required Test Equipment

Equipment	Description
Digital multimeter (DMM)	Fluke Model 87 or equivalent
Sensor extension cable	EC-8
Durasensor® oxygen transducer	DS-100A
Oxisensor® *II* oxygen transducer	D-25
ECG cable	CE-10
ECG electrodes	standard
ECG leads	LE series
NIBP hose	SHBP-10
NIBP cuff	SCBP series
Pulse oximeter tester	Nellcor SRC-2
ECG simulator	medSim 300 or equivalent
NIBP simulator	Bio-Tek “BP Pump” or equivalent
Respiration simulator	medSim 300 or equivalent
Temperature simulator	medSim 300 or equivalent
Safety analyzer	Bio-Tek 601 Pro or equivalent
Stopwatch	Manual or electronic

3.3 PERFORMANCE TESTS

The battery charge and battery performance test should be performed before monitor repairs whenever the battery is suspected as being a source of the problems. All other tests may be used following repairs or during routine maintenance (if required by your local institution. Before performing the battery performance test, ensure that the battery is fully charged (Paragraph 3.3.1).

This section is written using Nellcor factory-set power-up defaults. If your institution has preconfigured custom defaults, those values will be displayed.

3.3.1 Battery Charge

Perform the following procedure to fully charge the battery.

1. Connect monitor to AC power source using proper power cord.

2. Verify BATTERY CHARGING/AC SOURCE indicator is lit.

3. Charge battery for at least 8 hours.

Note: The battery may require a complete charge/discharge cycle to restore its normal capacity, depending on its previous usage.

4. The only way to check for a full charge is to perform the procedure in paragraph 3.3.2 "Battery Performance Test."

3.3.2 Battery Performance Test

1. The NPB-4000 monitor is specified to typically operate on battery power a minimum of 4 hours, at 25° C, with no printing, and one NIBP measurement every 15 minutes. The NPB-4000/C monitor is specified to typically operate on battery power a minimum of 3 hours, at 25° C, with no printing, and one NIBP measurement every 15 minutes. Before performing this test, ensure that the battery is fully charged (paragraph 3.3.1).

2. Connect *Nellcor* SRC-2 pulse oximeter tester to monitor viaEC-8 sensor cable.

3. Connect NIBP simulator to monitor via SHBP-10 hose.

4. Set SRC-2 switches as follows:

SWITCH	**POSITION**
RATE	38
LIGHT	LOW
MODULATION	LOW
RCAL/MODE	RCAL 63/LOC

5. Set NIBP simulator to simulate pressure setting of 120/80 mmHg and heart rate of 80 bpm.

6. Ensure monitor is not connected to AC power.

7. With NPB-4000/C turned off, press On/Standby switch and verify battery icon appears at bottom of display after power-on self-test is completed. Boxes in battery icon should all be filled, indicating battery is charged.

8. Verify monitor is responding to SpO_2 simulator signal and audible alarm is sounding. Use knob to select SpO_2 Menu and permanently silence SpO_2 audible alarm.

9. Use knob to select NIBP Menu and set Automatic Measurement Interval to 15 minutes. Exit menu and press front panel NIBP Start/Stop switch to manually initiate first NIBP measurement. Subsequent NIBP measurements will be taken automatically every 15 minutes.

10. NPB-4000 monitor must operate for at least 4 hours before monitor automatically powers down due to low battery condition. NPB-4000/C monitor must operate for at least 3 hours before monitor automatically powers down due to low battery condition.

11. Verify low battery alarm occurs 15-30 minutes before battery fully discharges.

12. Allow monitor to operate until it automatically powers down due to low battery condition. Verify audible alarm sounds when monitor automatically shuts down. Press Alarm Silence switch to terminate this audible alarm.

13. If monitor passes this test, immediately recharge battery (paragraph 3.3.1, steps 1–3).

3.3.3 Power-On Self-Test

1. Connect monitor to AC power source and verify BATTERY CHARGING/AC SOURCE indicator is lit.

2. Do not connect any input cables to monitor.

3. Observe monitor front panel. With monitor off, press On/Standby switch. Monitor must perform the following sequence.

    a. Monitor emits three consecutively higher pitched beeps.

    b. A few seconds later, display backlight illuminates, but display is blank.

    c. Nellcor logo then appears for a few seconds, with version numbers of boot and operational software displayed in lower left corner of display.

Note: The upper version number corresponds to the boot software, the lower version number corresponds to the operational software.

Note: Power-on self-test takes approximately 10 seconds to complete.

d. A beep signals end of power-on self-test

e. Upon successful completion of power-on self-test, display will be in normal monitoring screen configuration.

Note: No vital signs numeric values or waveforms will be displayed.

3.3.4 Hardware and Software Tests

Hardware and software testing include the following tests.

- 3.3.4.1 SpO_2 Testing
- 3.3.4.2 Operation with an ECG Simulator
- 3.3.4.3 Operation with a Respiration Simulator
- 3.3.4.4 Verification of Pneumatic System
- 3.3.4.5 Operation with a Temperature Simulator
- 3.3.4.6 General Operation

3.3.4.1 SpO_2 Testing

SpO_2 testing includes the following tests.

- 3.3.4.1.1 Alarms and Alarm Silence
- 3.3.4.1.2 Heart Rate Tone Volume Control
- 3.3.4.1.3 Dynamic Operating Range
- 3.3.4.1.4 LED Excitation Test

3.3.4.1.1 Alarms and Alarm Silence

1. Connect SRC-2 pulse oximeter tester to sensor input cable and connect cable to monitor.

2. Set SRC-2 as follows:

SWITCH	**POSITION**
RATE	38
LIGHT	LOW
MODULATION	OFF
RCAL/MODE	RCAL 63/LOCAL

3. Press monitor On/Standby switch to turn monitor on.

4. After normal power-up sequence, verify SpO_2% display initially indicates zero.

Note: The pulse bar may occasionally indicate a step change as the monitor is in the pulse search mode.

5. Move modulation switch on SRC-2 to LOW.

6. Verify following monitor reaction:

   a. Pulse bar begins to track artificial pulse signal from SRC-2.

   b. Initially, zero is displayed in SpO_2 frame.

   c. After about 10 to 20 seconds, monitor displays saturation and heart rate as specified by tester. Verify values are within following tolerances:

      Oxygen Saturation Range 79% to 83%

      Heart Rate Range 35 to 41 bpm

   d. Audible alarm sounds and both SpO_2% and HEART RATE displays will flash, indicating both parameters have violated default alarm limits.

   Note: Heart rate tone source, found in the Heart Rate Menu, should be set to "SpO_2".

   e. Heart rate tone is heard.

5. Press Alarm Silence switch on monitor front panel. Audible alarm is temporarily silenced.

6. Verify the following:

    a. An audible alarm remains silenced.

    b. "Slashed bell" icon appears in each numeric frame on display.

    c. SpO_2% and HEART RATE displays continue flashing.

    d. Heart rate tone is audible.

    e. Audible alarm returns in approximately 60 seconds.

3.3.4.1.2 Heart Rate Tone Volume Control

1. Set up NPB-4000/C monitor and SRC-2 pulse oximeter tester as indicated in paragraph 3.3.4.1.1.

2. Apply power to monitor and verify SpO_2 and heart rate values are correctly displayed.

3. Press Alarm Silence switch on front panel of the monitor to temporarily silence audible alarm.

4. Verify heart rate tone source, found in Heart Rate Menu, is set to "SpO_2".

5. Press Heart Rate Tone Volume switch on front panel of monitor.

6. Within 3 seconds of having pressed Heart Rate Tone Volume switch, rotate knob CW and verify beeping heart rate tone sound level increases.

7. Rotate knob CCW and verify beeping heart rate tone decreases until it is no longer audible.

8. Rotate knob CW to return beep volume to a comfortable level.

Note: Three seconds after the last switch-press or rotation of the knob, function of the knob reverts to moving the highlight on the display screen.

3.3.4.1.3 Dynamic Operating Range

The following test sequence verifies proper monitor operation over a range of input signals.

1. Connect SRC-2 to NPB-4000/C and turn NPB-4000/C on.

2. Place SRC-2 in RCAL 63/LOCAL mode.

3. Set SRC-2 as indicated in Table 3-2. Verify NPB-4000/C readings are within indicated tolerances. Allow monitor several seconds to stabilize readings.

Note: A "*" indicates values that produce an alarm. Press the Alarm Silence switch to temporarily silence the audible alarm.

Table 3-2: Dynamic Operating Range

SRC-2 Settings			NPB-4000/C Indications	
RATE	**LIGHT**	**MODULATION**	**SpO_2**	**Pulse Rate**
38	HIGH2	LOW	79 - 83*	35 - 41*
112	HIGH1	HIGH	79 - 83*	109 - 115
201	LOW	LOW	79 - 83*	195 - 207*
201	LOW	HIGH	79 - 83*	195 - 207*

Note: For the pulse rate setting of 201 BPM, the pulse rate tolerance of 195 to 207 BPM is greater than the ±3 BPM accuracy specification of the monitor, due to the performance characteristics of the SRC-2 tester.

4. Turn monitor off.

3.3.4.1.4 LED Excitation Test

This procedure uses normal system components to test circuit operation. A *Nellcor Oxisensor II* oxygen transducer, model D-25, is used to examine LED intensity control. The red LED is used to verify intensity modulation caused by the LED intensity control circuit.

1. Connect EC-8 sensor extension cable to monitor.
2. Connect D-25 sensor to sensor extension cable.
3. Press On/Standby switch to turn monitor on.
4. Leave sensor open with LEDs and photodetector visible.
5. After monitor completes normal power-up sequence, verify sensor LED is brightly lit.
6. Slowly move sensor LED in proximity of photodetector element of sensor. Verify; as LED approaches optical sensor, LED intensity decreases.
7. Open sensor and notice LED intensity increases.
8. Repeat step 6 and intensity will again decrease. This variation is an indication that microprocessor is in proper control of LED intensity.
9. Turn NPB-4000/C off.

3.3.4.2 Operation with an ECG Simulator

1. With monitor off, connect ECG leads to appropriate jacks on ECG tester.
2. Connect leads to CE-10 ECG cable.
3. Connect CE-10 to ECG input port on NPB-4000/C.
4. Set ECG tester as follows:

Heart rate:	30 bpm
Amplitude:	1 millivolt
Lead select:	II
Normal sinus rhythm	
Adult mode	

Note: The accuracy of NPB-4000/C ECG measurements is ±5 bpm. In the procedure below, add the tolerance of the simulator to the acceptable range of readings.

5. Press On/Standby switch to turn monitor on.
6. After normal power-up sequence, verify the following monitor reactions:
   a. After at least five heartbeats, monitor displays a heart rate of 30 ±5 bpm.
   b. Audible alarm will sound and HEART RATE display will flash, indicating heart rate is below default lower alarm limit.
7. Press Alarm Silence switch. Verify audible alarm is silenced.
8. Increase heart rate setting on ECG simulator to 240 bpm.
9. After at least five heartbeats, verify monitor displays heart rate of 240 ±5 bpm.
10. Verify audible alarm sounds and HEART RATE display flashes, indicating heart rate is above default upper alarm limit.
11. Press Alarm Silence switch to silence alarm.
12. Decrease heart rate setting on ECG simulator to 120 bpm.
13. After at least five heartbeats, verify monitor displays heart rate of 120 ±5 bpm.

14. Disconnect LL lead from ECG simulator.

15. Verify "Leads Off" alarm message appears, three dashes are displayed in HEART RATE display, and low priority audible alarm sounds.

16. Reconnect LL lead to ECG simulator. Verify "Leads Off" alarm message no longer appears and audible alarm is silenced.

17. Repeat steps 14 through 16 for LA and RA leads.

18. Turn monitor off.

3.3.4.3 Operation with a Respiration Simulator

1. With monitor off, connect ECG leads to appropriate jacks on respiration simulator.

2. Connect ECG leads to CE-10 ECG cable.

3. Connect CE-10 to ECG input port on NPB-4000/C.

Note: The accuracy of NPB-4000/C ECG measurements is ±3 breaths per minute. In the procedure below, add the tolerance of the simulator to the acceptable range of readings.

4. Set simulator for respiration rate of 120 breaths per minute.

5. Press On/Standby switch to turn monitor on.

6. After normal power-up sequence, verify the following monitor reactions:

   a. Monitor displays respiration rate of 120 ±3 breaths per minute.

   b. Audible alarm will sound and RESPIRATION RATE display will flash, indicating respiration rate is above default upper alarm limit.

7. Press Alarm Silence switch. Verify alarm is silenced.

8. Decrease respiration rate setting on respiration simulator to 20 breaths per minute.

9. Verify monitor displays respiration rate of 20 ±3 breaths per minute.

3.3.4.4 Verification of Pneumatic System

Tests in paragraphs 3.3.4.4.1 through 3.3.4.4.5 verify the functionality of the NPB-4000/C pneumatic system. These tests are designed to use the Bio-Tek "BP Pump" noninvasive blood pressure simulator. The internal test volume of the Bio-Tek simulator is 250 cm^3, which is used to calculated the inflation/deflation rate periods. The Bio-Tek simulator or any equivalent NIBP simulator is required to perform these tests.

The NPB-4000/C must be placed in Diagnostic Mode, with the NIBP Test screen active for each of the NIBP tests. For a detailed explanation of the Diagnostic Mode, refer to Section 4, **Power-up Defaults Menu and Diagnostic Mode**.

Each of the tests described in paragraphs 3.3.4.4.1 through 3.3.4.4.5 must be performed to verify pneumatic system functionality. These tests can be performed individually (in any order) or sequentially. Prior to performing any of these tests, perform the following setup procedure. If these tests are performed in sequence, this procedure needs to be performed once prior to the first test.

1. Turn on Bio-Tek simulator and press MODE button to place simulator in test mode. Simulator screen will indicate "Internal Cuff" and "Pressure Gauge".

2. Connect simulator hose to NIBP connector on NPB-4000/C.

3. Follow procedure described in Section 4 to place NPB-4000/C in Diagnostic Mode with NIBP Test screen active.

3.3.4.4.1 Pressure Transducer Accuracy

The pressure transducer accuracy test verifies the pressure accuracy of the NBP-4000/C pressure transducer.

1. Ensure Bio-Tek simulator is in test mode. Simulator should display "Pressure Gauge".

2. Ensure simulator is set up for internal cuff.

3. Ensure NIBP Test screen is active on NPB-4000/C.

4. Press Alarm Silence switch on NPB-4000/C to ensure both valves are closed.

5. Perform offset adjustment so that simulator and NBP-4000/C both display a pressure of 0 mmHg.

    a. Press Contrast Adjust switch on NPB-4000/C,

    b. Press Zero button on the simulator.

6. Press Select button on simulator until simulator displays “Pressure Source Set Test Pressure”.

7. Use Up/Down buttons on simulator to adjust for 250 mmHg.

8. Press Start Pump button on simulator. The simulator will begin to pressurize.

Note: The current pressure in mmHg will be displayed on both the simulator and NPB-4000/C displays.

9. Allow 15-20 seconds for pressure to stabilize.

Note: The pressure displayed on the NPB-4000/C and the simulator should be within 5 mmHg of one another to successfully complete the test.

10. Press Stop Pump button on simulator to stop test.

11. Press and hold Heart Rate Tone Volume switch until NPB-4000/C displays pressure of 0 mmHg.

Note: Additional NIBP tests may be performed at this time. If no further NIBP tests are to be conducted, turn the NPB-4000/C off. Normal monitoring operation will return the next time the monitor is turned on.

3.3.4.4.2 Pneumatic Leakage

The pneumatic leakage test verifies the integrity of the pneumatic system. A timer/stop watch is required for this test.

1. Ensure Bio-Tek simulator is in test mode. The simulator should display “Pressure Gauge”.

2. Ensure simulator is set up for internal cuff.

3. Ensure NIBP Test screen is active on NPB-4000/C.

4. Press Heart Rate Tone Volume switch on NPB-4000/C to ensure both valves are closed.

5. Perform offset adjustment so simulator and NBP-4000/C both display a pressure of 0 mmHg.

    a. Press Contrast Adjust switch on NPB-4000/C,

    b. Press Zero button on simulator,

6. Press NIBP Start/Stop switch on NPB-4000/C to activate pump. Hold NIBP Start/Stop switch until NPB-4000/C displays pressure of approximately 250 mmHg.

7. Allow 15-20 seconds for pressure to stabilize.

8. Record pressure displayed on NPB-4000/C.

9. Initiate a 1-minute timer.

10. After 1 minute, record pressure displayed on NPB-4000/C.

Note: The test will have been successfully completed if the pressure has dropped by 6 mmHg, or less, during the 1-minute period.

11. Press and hold Heart Rate Tone Volume switch until NPB-4000/C displays a pressure of 0 mmHg.

Note: Additional NIBP tests may be performed at this time. If no further NIBP tests are to be conducted, turn the NPB-4000/C off. Normal monitoring operation will return the next time the monitor is turned on.

3.3.4.4.3 Inflation Rate

The inflation rate test verifies the inflation rate of the NPB-4000/C. A timer/stop watch is required for this test.

1. Ensure Bio-Tek simulator is in test mode. The simulator should display "Pressure Gauge".

2. Ensure simulator is set up for internal cuff.

3. Ensure NIBP Test screen is active on NPB-4000/C.

4. Press Heart Rate Tone Volume switch on NPB-4000/C to ensure both valves are closed.

5. Perform offset adjustment so simulator and NBP-4000/C both display a pressure of 0 mmHg.

    a. Press Contrast Adjust switch on NPB-4000/C,

    b. Press Zero button on simulator

6. Simultaneously press and hold NIBP Start/Stop switch on NPB-4000/C to activate pump, and start the timer.

7. Hold NIBP Start/Stop switch until NPB-4000/C displays a pressure of 280 mmHg., and stop timer.

Note: The test will have been successfully completed if the inflation time is between 1 and 6 seconds.

8. Press and hold Heart Rate Tone Volume switch until NPB-4000/C displays a pressure of 0 mmHg.

Note: Additional NIBP tests may be performed at this time. If no further NIBP tests are to be conducted, turn the NPB-4000/C off. Normal monitoring operation will return the next time the monitor is turned on.

3.3.4.4.4 Deflation Rate

The deflation rate test verifies the deflation rate of the NPB-4000/C. A timer/stop watch is required for this test.

1. Ensure Bio-Tek simulator is in test mode. The simulator should display "Pressure Gauge".

2. Ensure simulator is set up for internal cuff.

3. Ensure NIBP Test screen is active on NPB-4000/C.

4. Press Heart Rate Tone Volume switch on NPB-4000/C to ensure that both valves are closed.

5. Perform offset adjustment so that simulator and NBP-4000/C both display a pressure of 0 mmHg.

    a. Press Contrast Adjust switch on NPB-4000/C,

    b. Press Zero button on simulator, to

6. Press and hold NIBP Start/Stop switch on NPB-4000/C to activate pump.

7. Hold NIBP Start/Stop switch until NPB-4000/C displays a pressure of 280 mmHg.

8. Start 1 minute timer, and simultaneously press and hold Alarm Silence switch on NPB-4000/C.

Note: This will cause the pneumatic system to deflate at a rate of 3 mmHg/sec ±1.5 mmHg/sec.

9. After 1 minute, record pressure displayed on the NPB-4000/C.

Note: The test will have been successfully completed if the NPB-4000/C displays a pressure reading of 10 mmHg to 190 mmHg.

10. Press and hold Heart Rate Tone Volume switch until NPB-4000/C displays a pressure of 0 mmHg.

Note: Additional NIBP tests may be performed at this time. If no further NIBP tests are to be conducted, turn the NPB-4000/C off. Normal monitoring operation will return the next time the monitor is turned on.

3.3.4.4.5 Over-pressure

The over-pressure test verifies the functionality of the over-pressure relief system of the NPB-4000/C.

1. Ensure Bio-Tek simulator is in test mode. The simulator should display "Pressure Gauge".

2. Ensure simulator is set up for internal cuff.

3. Ensure NIBP Test screen is active on NPB-4000/C.

4. Press Heart Rate Tone Volume switch on NPB-4000/C to ensure both valves are closed.

5. Perform offset adjustment so simulator and NBP-4000/C both display a pressure of 0 mmHg.

    a. Press Contrast Adjust switch on NPB-4000/C,

    b. Press Zero button on simulator, to

6. Press Select button on simulator until simulator displays "Overpressure Test".

7. Press Start Test button on simulator.

Note: The simulator will pressurize the system until the monitor's over-pressure relief system activates. The simulator will display the pressure value that caused the NPB-4000/C over-pressure relief system to activate. The test will have been successfully completed if the simulator displays a pressure reading of 280 mmHg to 330 mmHg.

8. Press and hold Heart Rate Tone Volume switch to ensure NPB-4000/C displays a pressure of 0 mmHg.

Note: Additional NIBP tests may be performed at this time. If no further NIBP tests are to be conducted, turn the NPB-4000/C off. Normal monitoring operation will return the next time the monitor is turned on.

3.3.4.5 Operation with a Temperature Simulator

1. With monitor off, connect temperature cable (supplied with the temperature simulator) to appropriate connector on temperature simulator.
2. Connect temperature cable to temperature input port on NPB-4000/C.
3. Set temperature simulator as follows:

Temperature:	37°C (98.6°F)
Probe type:	YSI 400 series

Note: The accuracy of NPB-4000/C temperature measurements is ±0.1˚ C (±0.2˚F). In the procedure below, add the tolerance of the simulator to the acceptable range of readings.

4. Press On/Standby switch to turn monitor on.

5. After normal power-up sequence, verify temperature reads 37˚ ±0.1˚ C (98.6˚F ±0.2˚F if Fahrenheit is selected as temperature units.)

6. Turn monitor off.

3.3.4.6 General Operation

The following tests are an overall performance check of the system:

- 3.3.4.6.1 Operation with a Human Subject
- 3.3.4.6.2 Serial Interface Test

3.3.4.6.1 Operation with a Human Subject

Patient monitoring involves connecting the monitor to a human subject for a qualitative test.

1. Connect EC-8 sensor extension cable to monitor.

2. Connect *Nellcor Durasensor* oxygen transducer, model DS-100A, to sensor extension cable.

3. Clip DS-100A to subject as recommended in sensor directions for use.

4. Connect a CE-10 ECG cable to NPB-4000/C.

5. Connect ECG leads to cable.

6. Connect ECG electrodes to leads.

7. Apply ECG electrodes to subject according to leads and electrodes directions for use.

8. Connect SHBP-10 blood pressure hose to monitor.

9. Apply appropriate SCBP series blood pressure cuff to subject according to the cuff directions for use.

10. Press On/Standby switch to turn monitor on and verify monitor is operating.

11. Monitor should stabilize on subject's physiological signal in about 15 to 30 seconds.

12. Verify saturation and heart and respiration rates are reasonable for subject.

13. Press NIBP Start/Stop switch on front panel of monitor.

14. Verify that blood pressure values are reasonable for subject.

3.3.4.6.2 Serial Interface Test

Perform the following procedure to test the serial port voltages. The test is qualitative and will only verify that the serial interface port is powered correctly, and that the "nurse call" signal is operational. The serial connector is a male DB-9, located on the monitor's rear panel, identified with the RS-232 symbol.

1. Set up DMM with function set to "VDC" at a range of 10 volts.

2. Connect DMM negative lead to RS-232 connector pin 5 (GND), or shell of connector.

3. Connect DMM positive lead to the following pins, in turn, and verify voltage values listed in Table 3-3.

Note: Voltage for pin 9 will be that listed for the "no alarm" condition.

Table 3-3: Serial Port Voltages

Pin	Signal	Measurement (V)		
		Min	Type	Max
1	not used	-0.4	0.0	0.4
2	RXD <<<	-0.4	0.0	0.4
3	TXD >>>	-5.0	-9.0	-15.0
4	DTR >>>	-5.0	-9.0	-15.0
5	GND	-0.4	0.0	0.4
6	DSR <<<	-0.4	0.0	0.4
7	RTS >>>	-5.0	-9.0	-15.0
8	CTS <<<	-0.4	0.0	0.4
9	Alarm Out >>> (no alarm)	-5.0	-9.0	-15.0
9	Alarm Out >>> (alarm underway)	5.0	9.0	15.0

4. Connect *Nellcor* SRC-2 pulse oximeter tester to monitor via EC-8 sensor extension cable.

5. Set SRC-2 switches as follows:

SWITCH	**POSITION**
RATE	38
LIGHT	LOW
MODULATION	LOW
RCAL/MODE	RCAL 63/LOC

6. Verify monitor is responding to SpO_2 simulator signal and audible alarm is sounding.

Note: If desired, press the Alarm Silence switch to temporarily silence the audible alarm.

7. Connect DMM positive lead to pin 9 and verify voltage value listed in Table 3-3. (Voltage for pin 9 will be that listed for the "alarm underway" condition.)

3.4 SAFETY TESTS

NPB-4000/C safety tests meet the standards of, and are performed in accordance with, IEC 601-1, Clause 19 (EN60601-1, Second Edition, 1988; Amendment 1, 1991-11, Amendment 2, 1995-03) and UL 2601-1 (August 18, 1994), for instruments classified as Class 1 and TYPE CF and AAMI Standard ES1 (ANSI/AAMI ES1 1993).

- 3.4.1 Ground Integrity
- 3.4.2 Electrical Leakage

3.4.1 Protective Earth Continuity

This test checks the integrity of the power cord ground wire from the AC plug to the instrument chassis ground. The current used for this test is less than or equal to 6 Volts RMS, 50 to 60 Hz, and 25 Amperes.

1. Connect the monitor AC mains plug to the analyzer as recommended by the analyzer operating instructions.

2. Connect the analyzer resistance input lead to the equipotential terminal (ground lug) on the rear of the instrument. Verify that the analyzer indicates 100 milliohms or less.

3.4.2 Electrical Leakage

The following tests verify the electrical leakage of the monitor:

- 3.4.2.1 Earth Leakage Current
- 3.4.2.2 Enclosure Leakage Current
- 3.4.2.3 Patient Leakage Current
- 3.4.2.4 Patient Source Current (Mains on Applied Part)
- 3.4.2.5 Patient Auxiliary Current

3.4.2.1 Earth Leakage Current

This test is in compliance with IEC 601-1 (earth Leakage current) and AAMI Standard ES1 (earth risk current). The applied voltage for AAMI ES1 is 120 Volts AC, 60 Hz, for IEC 601-1 the voltage is 264 Volts AC, 50 to 60 Hz. All measurements shall be made with the power switch in both "On" and "Off" positions.

1. Connect the monitor AC plug to the electrical safety analyzer as recommended by the analyzer operating instructions.

2. Perform test as recommended by analyzer operating instructions.

Note: Earth leakage current is measured under various conditions of the AC mains and protective earth conductor. For each condition, the measured leakage current must not exceed that indicated in Table 3-4.

Table 3-4: Earth Leakage Current Values

Test Condition	Allowable Leakage Current (microamps)
Normal polarity	300
Normal polarity; Neutral (L2) open	1,000
Reverse polarity	300
Reverse polarity; Neutral (L2) open	1,000

3.4.2.2 Enclosure Leakage Current

This test is in compliance with IEC 601-1 (enclosure leakage current) and AAMI Standard ES1 (enclosure risk current). This test is for ungrounded enclosure current, measured between enclosure parts and earth. The applied voltage for AAMI/ANSI is 120 Volts AC at 60 HZ, and for IEC 601-1 the applied voltage is 264 Volts AC at 50 to 60 Hz.

1. Connect the monitor AC plug to the electrical safety analyzer as recommended by the analyzer operating instructions.

2. Place a 200 cm^2 foil in contact with the instrument case making sure the foil is not in contact with any metal parts of the enclosure that may be grounded.

3. Measure the leakage current between the foil and earth.

Note: The analyzer leakage current indication must note exceed the values listed in Table 3-5.

Table 3-5: Enclosure Leakage Current

AC Line Cord	Neutral Line Wire	Power Line Ground Wire	IEC 601-1	AAMI/ANSI ES1 Standard
Closed	Closed	Closed	100 µA	100 µA
Closed	Closed	Open	500 µA	300 µA
Closed	Open	Closed	500 µA	300 µA
Open	Closed	Closed	500 µA	100 µA
Open	Open	Closed	500 µA	300 µA
Open	Closed	Open	500 µA	300 µA

3.4.2.3 Patient Leakage Current

This test measures patient leakage current in accordance with IEC 601-1, clause 19, for Class I, type CF equipment. Patient leakage current in this test is measured from any individual patient connection to earth (power ground).

Note: This test requires a test cable for each patient connector. For example, the ECG test cable consists of the ECG cable connector, with all conductors shorted together, connected to a test lead from the electrical safety analyzer. Test cables for SpO_2 and temperature can be configured in a similar manner, by wrapping each sensor end individually with aluminum foil filled with conductive gel (only enough gel to ensure conductivity). Attach a wire to the foil that is connected to a test lead from the electrical safety analyzer.

1. Configure the electrical safety analyzer as recommended by the analyzer operating instructions.

2. Connect the monitor's AC mains power cord to the analyzer as recommended by the analyzer operating instructions.

3. Connect the ECG test cable between the ECG connector on the NPB- 4000/C and the appropriate input connector on the analyzer.

4. Turn on the NPB- 4000/C.

5. Perform the patient leakage current test as recommended by the analyzer operating instructions.

Note: Patient leakage current is measured under various conditions of the AC mains and protective earth conductor. For each condition, the measured leakage current must not exceed that indicated in Table 3-6.

6. Repeat the patient leakage current test for the SpO_2 and temperature patient connections, using the appropriate test cables.

Table 3-6: Patient Leakage Current Values

Test Condition	Allowable Leakage Current (microamps)
Normal polarity	10
Normal polarity; Neutral (L2) open	50
Normal polarity; Earth open	50
Reverse polarity	10
Reverse polarity; Neutral (L2) open	50
Reverse polarity; Earth open	50

3.4.2.4 Patient Leakage Current - (Mains Voltage on the Applied Part)

This test measures patient leakage current in accordance with IEC 601-1, clause 19, for Class I, type CF equipment. In this test, 110% of mains voltage is applied between each patient connection and earth (power ground). Patient leakage current is then measured from any individual patient connection to earth.

Note: This test requires the same test cables for each patient connector as described in paragraph 3.4.2.3.

Warning: AC mains voltage will be present on the applied part terminals during this test. Exercise caution to avoid electrical shock hazard.

1. Configure electrical safety analyzer as recommended by analyzer operating instructions.

2. Connect monitor's AC mains power cord to analyzer as recommended by analyzer operating instructions.

3. Connect ECG test cable between ECG connector on NPB-4000/C and appropriate input connector on analyzer.

4. Turn on NPB-4000/C.

5. Perform test as recommended by analyzer operating instructions.

Note: Patient leakage current is measured with normal and reverse mains polarity. For each condition, the measured leakage current must not exceed that indicated in Table 3-7

6. Repeat test for SpO_2 and temperature patient connections, using appropriate test cables.

Table 3-7: Patient Leakage Current Values—Mains Voltage on Applied Part

Test Condition	Allowable Leakage Current (microamps)
Normal polarity	50
Reverse polarity	50

3.4.2.5 Patient Auxiliary Current

This test measures patient auxiliary current in accordance with IEC 601-1, clause 19, for Class 1, type CF equipment.

The applied voltage for AAMI ESI is 120 volts, 60 Hz, and for IEC 601-1 the voltage is 264 volts, 50 to 60 Hz.

Patient auxiliary current is measured between each ECG test lead and between each sensor connection for all possible connections.

Note: This test requires the same test cables for each patient connector as described in paragraph 3.4.2.3.

1. Configure the electrical safety analyzer as recommended by the electrical analyzer's operating instructions.
2. Connect the monitor's AC mains power cord to the electrical analyzer as recommended by the electrical analyzer's operating instructions.
3. Connect the patient test lead combination in table 3-8 to the appropriate input connector on the electrical analyzer.
4. Turn on the NBP-4000/4000C.
5. Perform patient auxiliary current test per table 3-9 as recommended by electrical analyzer's operating instructions.
6. Repeat the patient auxiliary current test for each test lead combination as listed in Table 3-8 and measure each patient auxiliary current.

Table 3-8: Test Lead Combinations

First Test Lead	Second Test Lead
ECG # 1 (LA)	ECG # 2 (LL)
ECG #1 (LA)	ECG #3 (RA)
ECG #2 (LL)	ECG #3 (RA)
ECG #1 (LA)	Temperature
ECG #2 (LL)	Temperature
ECG #3 (RA)	Temperature
ECG #1 (LA)	SpO_2
ECG #2 (LL)	SpO_2
ECG #3 (RA)	SpO_2
Temperature	SpO_2

Table 3-9: Allowable Leakage Current

Polarity	Neutral Line Wire (L2)	Power Line Ground Wire	Allowable Leakage Current (microamps)
Normal	Closed	Normal	10
Normal	Open	Normal	50
Normal	Closed	Open	50
Reversed	Closed	Normal	10
Reversed	Open	Normal	50
Reversed	Closed	Open	50

SECTION 4: POWER-UP DEFAULTS MENU AND DIAGNOSTIC MODE

4.1 Introduction
4.2 Power-up Defaults Menu
4.3 Diagnostic Mode

4. POWER-UP DEFAULTS MENU AND DIAGNOSTIC MODE

4.1 INTRODUCTION

This section discusses use of the Power-up Defaults Menu to configure power-on default settings, and the Diagnostic Mode to obtain service-related information about the monitor.

4.2 POWER-UP DEFAULTS MENU

The purpose of the Power-up Defaults Menu (Table 4-1) is to allow the authorized user to create a "power-up default" for each setting in the NPB-4000/C. Power-up defaults are the settings in effect each time the NPB-4000/C is powered on. Once the Power-up Defaults Menu is entered, physiological monitoring is terminated. The screen layouts do not display any information associated with normal monitoring operation.

Use the following procedure to configure the power-up default settings for the NPB-4000/C monitor:

1. Set NPB-4000/C to normal monitoring mode.

2. Adjust each accessible setting on monitor as desired.

Note: Use the techniques described in the operator's manual. Such settings include alarm limits, choice of display type for the graphic frames, and ECG lead select.

3. Use knob to invoke Set-up Menu (choose the screwdriver icon found along the bottom of the display).

4. Select menu item "Enter Power-Up Defaults Menu".

Note: Once selected, a pop-up box will appear with the text "Enter 3-Digit Passcode". Use the knob to enter the passcode, 2 1 5. This passcode is set at the factory and may not be changed.

5. Enter Passcode. The Power-up Defaults Menu will now be present. The available menu items are explained in Table 4-1. Make changes to these menu items as desired.

Table 4-1: Power-up Defaults Menu

MENU ITEM	CHOICES	EXPLANATION
Accept Current Settings as Power-Up Defaults?	"Yes" "No"	If "Yes" is chosen, the current NPB-4000/C settings become the power-up defaults.
Adult/Neonatal Mode		Neonatal mode is not available at this time; thus, when this item is selected, the following pop-up message will appear: "Selection not available".
Permanent Audible Alarm Silence	"Make Available" "Deny Access"	If "Make Available" is chosen, the caregiver may permanently silence the audible alarm for a particular parameter via the Alarm/Limits Menu. Some institutions may wish to prevent audible alarms from being permanently silenced. If so, "Deny Access" should be selected.
Alarm Suspend	"Make Available" "Deny Access"	If "Make Available" is chosen, the caregiver may invoke the Alarm Suspend Mode by pressing and holding the Alarm Silence switch for 2 seconds. Some institutions may wish to prevent Alarm Suspend from being invoked. If so, "Deny Access" should be selected.
Auto-Set Limits	"Make Available" "Deny Access"	If "Make Available" is chosen, the caregiver may invoke the Auto-Set Limits function via the Alarm/Limits Menu. Some institutions may wish to prevent Auto-Set Limits from being invoked. If so, "Deny Access" should be selected.

Table 4-1: Power-up Defaults Menu

MENU ITEM	CHOICES	EXPLANATION
Language	"English" "French" "German" "Spanish" "Italian" "Portuguese" "Japanese" "Russian" "Chinese"	The language selected will be used for all the text shown on the display; the selected language will be effective the next time the monitor is powered up. *(Note that if an unfamiliar language is chosen, the user may find it difficult to operate the monitor.)*
Enter Diagnostic Mode	"Yes" "No"	If "Yes" is chosen, the Power-up Defaults Menu is exited and the Diagnostic Menu appears.
Done		When selected, the Power-up Defaults Menu is immediately exited and the user is instructed to power down the monitor.

6. After making changes to menu items, pick menu item "Accept current settings as power-up defaults?"

7. Select "YES".

8. Select "Done".

Upon selecting "Done", a Notice screen will appear, with the directions that the monitor must be powered off, and that any changes made to the power-up defaults will be in effect next time the unit is powered up.

4.3 DIAGNOSTIC MODE

The purpose of Diagnostic Mode is to allow factory, field-service and hospital biomedical technicians access to a series of test and system-related information screens for the purpose of verifying NPB-4000/C performance or troubleshooting problems.

To access the Diagnostic Mode, first invoke the Power-up Defaults Menu as described in paragraph 4.2. Then, select the menu item, "Enter Diagnostic Mode". Choose "Yes"; the Power-up Defaults Menu will be exited and the Diagnostic Menu will appear.

The Diagnostic Menu lists the test and system-related information screens. Selection of an item in the menu will invoke that test or information screen. The test and information screens that appear in the Diagnostic Menu are as follows:

- Error Codes
- System Information
- System A/D Values
- NIBP Test

4.3.1 Error Codes

This screen displays the 10 most recent error codes logged by the NPB-4000/C. After 10 error codes have been logged, the oldest error codes will be deleted as new error codes are added. The error code is displayed in hexadecimal. Adjacent to each error code will be the date/time when the error code was recorded. Error codes may not be changed or reset in this screen. When in the Error Code screen, the "Return" item is always highlighted; pressing the knob will return the user to the Diagnostic Menu. Rotating the knob, while in the Error Code screen, will have no effect.

Refer to paragraph 5.6.2 for more detail on error codes.

4.3.2 System Information

This screen displays several system-related items:

- **Monitor On-time**: Displays the number of hours, rounded to the nearest hour, that the Main PCB has been operational. This value may not be reset.

Note: The **Monitor On-time** value is stored in nonvolatile memory located in the real-time clock chip, when a new Main PCB is installed, this value will be reset to zero.)

- **Backlight On-time**: Displays the number of hours, rounded to the nearest hour, that the LCD Backlight has been operational. This value may be reset to zero, for instance at the time when a technician changes the backlight or installs a new LCD.

- **Recorder On-time**: Displays the number of hours, rounded to the nearest hour, that the Recorder has been operational. This value may be reset to zero, for instance at the time when a technician installs a new recorder.

- **Battery Deep Discharges**: Displays the number of deep-discharge cycles seen by the battery. The monitor records a deep discharge cycle when the battery voltage reaches 5.6 volts, the voltage at which a "Low Battery" alarm is issued. This value may be reset to zero, for instance at the time when a technician installs a new battery.

- **System Software Version**: Displays the revision level of the system software. The revision level is also momentarily shown on the LCD as part of the Copyright screen. This value may not be changed by the user.

- **SpO2 Software Version**: Displays the revision level of the software of the MP-205 SpO2 module. This value may not be changed by the user.

When in the System Information screen, the knob may be rotated to select any of the "changeable" items. If one of those items is selected, a press of the knob will cause a pop-up menu to appear. The first item in the pop-up will read "Make no change"; the second item in the pop-up will read "Reset to zero". Exiting the screen is accomplished in the normal manner, by selecting "Return".

4.3.3 System A/D Values

This screen displays the current value of each analog-to-digital (A/D) channel, in volts. Some of the channels are for AC-coupled signals (such as ECG input), so the numbers on the screen will be constantly changing when an input signal is present. These AC-coupled values are shown to give an indication as to whether basic functionality of the channel is present, but no significance can be derived from the values of the numbers displayed. However, others of the A/D channels read DC voltages, (for example, power supply voltages and battery voltage) those voltage values directly provide useful diagnostic information.

The Primary and Secondary Status messages from the SpO2 module will be displayed and updated at the rate of about once per second. Presence of the correct SpO2 message indicates that, at a basic level, communication between the SpO2 module and the main monitor processor is working correctly. None of the displayed values may be changed or reset in this screen.

When in the System A/D screen, the "Return" item is always highlighted; a press of the knob will return the user to the Diagnostic Menu. Rotating the knob while in the System A/D screen will have no effect. The A/D channel designators are shown in Table 4-2.

Table 4-2: A/D Channel Designators

A/D CHANNEL DESIGNATOR		A/D CHANNEL DESIGNATOR	
1.	ECG	12.	(BATTERY VOLTAGE) X 0.5
2.	RWAVE	13.	not used
3.	PACEMAKER	14.	+3.3VDC POWER SUPPLY
4.	RESPIRATION	15.	(+12VDC POWER SUPPLY) X 0.33
5.	PRESSURE XDUCER 1	16.	(NIBP VOLTAGE REF) X 0.8
6.	PRESSURE XDUCER 2	17.	GROUND REFERENCE
7.	NIBP OSCILLATORY	18.	(+5 VDC POWER SUPPLY) X 0.8
8.	ECG LEADS OFF	19.	ADC MID-SCALE VALUE
9.	TEMERATURE	20.	ADC FULL-SCALE VALUE
10.	ISOLATED VOLTAGE REF	21.	ADC ZERO-SCALL VALUE
11.	ISOLATED VOLTAGE ZERO		
	SpO2 S1 S018		SpO2 S2 S010

4.3.4 NIPB Test

An NIBP Test screen is provided to facilitate troubleshooting problems and performing verification testing for the NIBP subsystem. Typically, when these tests are performed, the pneumatic system is connected to an external pressure-reading device and a closed reference volume. The NIBP Test screen provides a real-time numeric display of the pressure in the pneumatic system, means for controlling the pump and valves, and a display indicating whether the proportional and safety valves are open or closed.

Warning: A blood pressure cuff, connected to the monitor, should never be applied to a human subject while the monitor is in Diagnostic Mode, as injury could result.

The NIBP Test screen elements are described below:

- **Pressure Display**: The real-time value of the system pneumatic pressure is displayed in mmHg. The value is updated at the rate of approximately two times per second.

- **Proportional Valve Display**: The display indicates whether the proportional valve is open or closed.

- **Safety Valve Display**: The display indicates whether the safety valve is open or closed.

- **Activate pump**: For as long as the NIBP Start/Stop switch is pressed, the pump will run. If system pressure reaches the hardware over-pressure protection point (280 to 330 mmHg), the safety valve will open and the pump will be disabled, until the pressure falls below the safety threshold.

- **Deflate**: For as long as the Alarm Silence switch is pressed, the proportional valve will open and bleed off pressure at the rate of 3 ±1.5 mmHg/sec.

- **Open Both Valves**: For as long as the Heart Rate Tone Volume switch is pressed, the safety valve and proportional valve open to maximum and remain so for as long as the switch is pressed.

- **Offset Adjust**: A momentary press of the Contrast Adjust switch will invoke the "zero calibration" routine that is performed immediately prior to each blood pressure measurement. This routine looks at the pressure in the system, and if the pressure is non-zero, an offset is applied which causes the system pressure to be displayed as "zero".

- When in the NIBP Test screen, the "Return" item is always highlighted; a press of the knob will return the user to the Diagnostic Menu. Rotating the knob while in the NIBP Test screen will have no effect.

SECTION 5: TROUBLESHOOTING

5.1 Introduction
5.2 How to Use this Section
5.3 Who Should Perform Repairs
5.4 Replacement Level Supported
5.5 Obtaining Replacement Parts
5.6 Troubleshooting Guide

5. TROUBLESHOOTING

5.1 INTRODUCTION

This section explains how to troubleshoot the NPB-4000/C if problems arise. Tables are supplied that list possible monitor difficulties, along with probable causes, and recommended actions to correct the difficulty.

5.2 HOW TO USE THIS SECTION

Use this section in conjunction with Section 3, **Performance Verification**, and Section 7, **Spare Parts**. To remove and replace a part you suspect is defective, follow the instructions in Section 6, **Disassembly Guide**. The circuit analysis section in the Technical Supplement appendix offers information on how the monitor functions.

5.3 WHO SHOULD PERFORM REPAIRS

Only qualified service personnel should open the monitor housing, remove and replace components, or make adjustments. If your medical facility does not have qualified service personnel, contact Mallinckrodt Technical Services or your local Mallinckrodt representative.

5.4 REPLACEMENT LEVEL SUPPORTED

The replacement level supported for this product is to the printed circuit board (PCB) and major subassembly level. Once you isolate a suspected PCB, follow the procedures in Section 6, **Disassembly Guide**, to replace the PCB with a known good PCB. Check to see if the trouble symptom disappears and that the monitor passes all performance tests. If the trouble symptom persists, swap back the replacement PCB with the suspected malfunctioning PCB (the original PCB that was installed when you started troubleshooting) and continue troubleshooting as directed in this section.

5.5 OBTAINING REPLACEMENT PARTS

Mallinckrodt Technical Services provides technical assistance information and replacement parts. To obtain replacement parts, contact Mallinckrodt or your local Mallinckrodt representative. Refer to parts by the part names and part numbers listed in Section 7, **Spare Parts**.

5.6 TROUBLESHOOTING GUIDE

Problems with the NPB-4000/C are separated into the categories indicated in Table 5-1. Refer to the paragraph indicated for further troubleshooting instructions.

Note: Taking the recommended actions discussed in this section will correct the majority of problems you will encounter. However, problems not covered here can be resolved by calling Mallinckrodt Technical Services or your local Mallinckrodt representative.

Table 5-1: Problem Categories

Problem Area	Refer to Paragraph
1. Power • No power-up • Fails power-on self-test • Powers down without apparent cause	5.6.1
2. Error Messages	5.6.2
3. Switches/Knob • Monitor does not respond properly to switches	5.6.3
4. Display/Audible Tones • Display does not respond properly • Tones do not sound properly	5.6.4
5. Operational Performance • Displays appear to be operational, but monitor shows no readings • Suspect readings • Printer not responding	5.6.5

All of the categories in Table 5-1are discussed in the following paragraphs.

5.6.1 Power

Table 5-2 lists recommended actions to address power problems.

Table 5-2: Power Problems

Condition	Recommended Action
1. The NPB-4000/C fails to power-up when the On/Standby switch is pressed.	1. Ensure power cord is plugged into operational AC outlet of appropriate voltage and frequency. Ensure green BATTERY CHARGING/AC SOURCE indicator is lit. If indicator is not lit, replace power supply assembly. 2. Check fuses located on power supply assembly above AC inlet receptacle. Replace fuses if necessary. 3. Inside monitor, check main ribbon cable and ensure that it is connected to main PCB and power supply assembly. 4. Ensure keypad is plugged into Main PCB. If connection is good, replace keypad. 5. If the problem persists, replace main PCB.
2. The NPB-4000/C turns on, then shuts off and sounds an alarm and no error code is displayed.	1. Press Alarm Silence switch to terminate audible alarm. Ensure AC power cord is connected and green BATTERY CHARGING/AC SOURCE indicator is lit, or ensure DC source is connected and green BATTERY CHARGING/DC SOURCE indicator is lit. If monitors operates successfully, battery may be discharged. 2. Recharge battery as directed in paragraph 3.3.1. If battery fails to hold charge, replace battery. 3. If problem persists, replace main PCB. 4. If problem persists, replace power supply assembly.

5.6.2 Error Codes

When the NPB-4000/C detects an error condition, the monitor will attempt to show an error code on the display screen. If such an error occurs during monitoring operation, an audible alarm tone will sound. Press the Alarm Silence switch to terminate the audible alarm tone.

Error codes are displayed in hexadecimal numbers. Additionally, Diagnostic Mode may be used to gain access to an error code record, stored in non-volatile memory, of the last 10 error codes encountered by the monitor. Refer to Section 4 for further details on Diagnostic Mode.

Each error code corresponds to a particular problem in the monitor. Listed in the sections that follow are recommended actions to take when an error code is encountered.

5.6.2.1 Serviceable Hardware Error Codes

Listed in **Error! Reference source not found.** are error codes that correspond to hardware problems, and the recommended actions to take should such an error be encountered.

Table 5-3: Serviceable Hardware Error Codes

Hex Code	Explanation	Recommended Action
1	Improper shutdown.	1. Cycle power. 2. If error persists, return monitor for service.
2	NIBP Sensor Error. • The two pressure transducers do not agree.	1. Check for blocked hoses in pneumatic system. 2. Replace main PCB
3	NIBP Pressure Violation Error. • Pressure on cuff could not be removed by normal means. • A fault has been detected in NIBP system that could not be handled by releasing pressure by normal means. • NIBP system has released pressure using safety valve.	1. Cycle power. 2. Check for blocked hoses in pneumatic system. 3. Replace main PCB. Note: This error may occur during a blood pressure measurement in STAT mode, if the leg cuff is used.
4	Measured value of 3.3-volt power supply was low.	1. Check power supply. 2. Replace power supply assembly.
5	Measured value of 3.3-volt power supply was high.	1. Check power supply. 2. Replace power supply assembly.
6	Measured value of 12-volt power supply was low.	1. Check power supply. 2. Replace power supply assembly.
7	Measured value of 12-volt power supply was high.	1. Check power supply. 2. Replace power supply assembly.
8	Measured value of 5-volt power supply was low.	1. Check power supply. 2. Replace power supply assembly.
9	Measured value of 5-volt power supply was high.	1. Check power supply. 2. Replace power supply assembly.

Table 5-3: Serviceable Hardware Error Codes

Hex Code	Explanation	Recommended Action
A	Measured value of isolated reference supply on front end was low	1. Check power supply. 2. Replace main PCB.
B	On a NPB-4000 rev 4 PCB or earlier. The measured value of isolated reference supply on front end was high.	1. Check power supply. 2. Replace main PCB.
C	On a NPB-4000 rev 5 or later, or on NPB-4000C. The measured value of isolated reference supply on front end was high.	1. Check power supply. 2. Replace main PCB.
64	MP-205 SpO_2 module is not sending messages to host CPU.	1. Ensure MP-205 module is properly connected. 2. Replace MP-205 module. 3. If problem persists, replace main PCB.
65, 66	MP-205 SpO_2 module has detected an error during initialization.	1. Replace MP-205 module. 2. If problem persists, replace main PCB.
6E-71	MP-205 SpO_2 module has detected an error on its serial port.	1. Replace MP-205 module. 2. If problem persists, replace main PCB.

5.6.2.2 Other Error Codes

If an error code occurs that is not listed in paragraph 5.6.2.1, take the following actions:

1. Turn monitor off, then on again.

2. If error code still appears, take monitor out of service and contact Mallinckrodt Technical Services or your local Mallinckrodt representative for advice on remedial action.

3. If monitor powers up and error code does not recur, enter Diagnostic Mode and invoke Error Code screen. Examine record of last 10 error codes and determine if same error code had occurred previously.

4. If Error Code screen indicates same error has occurred previously, take monitor out of service and contact Mallinckrodt Technical Services or your local Mallinckrodt representative for advice on remedial action.

5. If Error Code screen indicates no previous occurrences of this error, monitor may be returned to service.

As a reference, Table 5-4 lists the general categories for other error codes. The error code categories are shown only in hexadecimal format:

Table 5-4: Error Code Categories

Code (hex)	Explanation
500xxxx	internal user interface error
501xxxx	remote serial port error
502xxxx	date and time error
503xxxx	NIBP error
504xxxx	front end error
505xxxx	alarm error
506xxxx	audio error
507xxxx	recorder error
508xxxx	trend error
509xxxx	flash memory data error
50axxxx	SpO_2 error
50bxxxx	ECG error
50cxxxx	power down task error
50dxxxx	on board diagnostic error
50exxxx	power monitor error
50fxxxx	temperature measurement error
510xxxx	internal user interface error
511xxxx	error handling error
512xxxx	pSOS (operating system) initialization error
513xxxx	serial driver error

5.6.3 Switches/Knobs

Table 5-5 lists recommended actions to address problems with the knob and front panel switches.

Table 5-5: Switches/Knob Problems

Condition	Recommended Action
1. NPB-4000/C fails to power-up when On/Standby switch is pressed.	1. Take steps as noted in paragraph 5.6.1.
2. NPB-4000/C powers-up, but some or one of the other switches respond.	1. Ensure keypad is plugged into Main PCB. If connection is good, change keypad. 2. If problem persists, change Main PCB.
3. When knob is rotated, no highlight appears on display screen, and/or monitor does not respond to knob presses.	1. Ensure encoder cable is plugged into Main PCB. If connection is good, change encoder. 2. If problem persists, replace Main PCB.

5.6.4 Display/Audible Tones

Table 5-6 lists recommended actions to address problems with the display and audible tones.

Table 5-6: Display/Audible Tones Problems

Condition	Recommended Action
1. System powers-up and… • LCD screen is totally black or white. Or, • LCD screen is illuminated, but no data is visible. Or, • LCD screen has data, but is not illuminated.	Note: Pressing the NPB-4000 contrast adjust switch causes the LCD contrast setting to immediately change to normal, factory-default value. Pressing the NPB-4000/C contrast adjust switch toggles the display between the two different color schemes (black background and white background). 1. NPB-4000. Adjust LCD screen contrast by pressing contrast adjust switch momentarily, then turning knob four revolutions in each direction. Turning knob counter-clockwise should brighten screen; turning knob clockwise should darken screen. Or 2. NPB-4000C. Adjust LCD screen contrast by pressing contrast adjust switch momentarily. Screen will toggle background color. 3. Ensure red LED, located on top left corner of main PCB is illuminated. If LED is not illuminated, monitor is not in “on” state; follow troubleshooting steps in paragraph 5.6.1. 4. Ensure backlight cable is connected to main PCB and backlight inverter PCB. 5. Ensure LCD cable is connected to main PCB and LCD PCB. 6. If problem persists, replace main PCB. 7. If problem persists, replace backlight PCB. 8. If problem persists, replace LCD assembly.
2. NPB-4000/C responds to switch press, but key press tone fails to sound.	1. Ensure speaker cable is connected to power supply assembly. 2. If problem persists, replace speaker assembly. 3. If problem persists, replace main PCB.

Table 5-6: Display/Audible Tones Problems

Condition	Recommended Action
3. Audible alarm does not sound.	1. Verify alarm volume setting in Alarm/Limits menu, and test operation of alarm tone by pressing Heart Rate Tone Volume switch while alarm volume setting is displayed. 2. Ensure speaker cable is connected to power supply assembly. 3. If problem persists, replace speaker assembly. 4. If problem persists, replace main PCB.

5.6.5 Operational Performance

Table 5-7 lists recommended actions to address problems related to operational performance.

Table 5-7: Operational Performance Problems

Condition	Recommended Action
1. Monitor appears to be operational, but physiological values are suspect or nonexistent.	1. Replace each patient cable (or hose) with a known serviceable cable. 2. Ensure internal ECG, temperature, and SpO_2 cables are connected to main PCB. Ensure hoses in pneumatic system are properly connected, and NIBP pump motor is connected to power supply PCB. 3. If problem persists, replace main PCB.
2. Printer paper will not advance.	1. Open printer door and check paper is present. Press printer module firmly into monitor to ensure printer module is fully engaged with connector on printer PCB. 2. Cycle power on monitor. Printer should execute a line feed at conclusion of power-up sequence. 3. If problem persists, ensure main ribbon cable is connected to printer PCB, power supply, and main PCB. 4. If problem persists, replace printer. 5. If problem persists, replace printer PCB. 6. If problem persists, replace main PCB.

Table 5-7: Operational Performance Problems

Condition	Recommended Action
3. Printer paper will advance, but paper remains blank when printing should be present.	1. Open printer door and check paper is oriented correctly; paper should exit from bottom of roll. See operator's manual for an illustration of correct paper orientation. 2. If problem persists, replace printer.

SECTION 6: DISASSEMBLY GUIDE

6.1 Introduction
6.2 How to Use this Section
6.3 Disassembly Sequence Flow Charts
6.4 Closed Case Disassembly Procedures
6.5 Front Case Disassembly Procedures
6.6 Rear Case Disassembly Procedures

6. DISASSEMBLY GUIDE

WARNING: Performance Verification. Do not place the NPB-4000/C into operation after repair or maintenance has been performed, until all Performance Tests and Safety Tests listed in Section 3 of this service manual have been performed. Failure to perform all tests could result in erroneous monitor readings.

6.1 INTRODUCTION

The NPB-4000/C can be disassembled down to all major component parts, including:

- PCBs
- battery
- cables
- function switches
- chassis enclosures

The following tools are required:

- small, Phillips-head screwdriver
- medium, Phillips-head screwdriver
- needle-nose pliers
- 9/16-inch socket (for knob encoder)

WARNING: Before attempting to open or disassemble the NPB-4000/C, disconnect the power cord from the NPB-4000/C.

Caution: Observe ESD (electrostatic discharge) precautions when working within the unit.

Note: Some spare parts have a business reply card attached. When you receive these spare parts, please fill out and return the card.

6.2 HOW TO USE THIS SECTION

The step-by-step procedures that are used to access replaceable parts of the NPB-4000/C are illustrated in the Disassembly Sequence Flow Charts in paragraph 6.3, Figure 6-1 and Figure 6-2. As indicated in the flow charts, the monitor consists of two main assemblies, the Front Case Assembly and Rear Case Assembly.

The ovals on the flow charts contain reference designators that point to specific steps in the Disassembly Procedures. The Disassembly Procedures, paragraphs 6.4, 6.5, and 6.6 contain detailed disassembly instructions, accompanied by illustrations.

The rectangular boxes on the flow charts represent the various components or sub-assemblies. The digits appearing in these boxes are the part numbers of the component or subassembly. Section 7, **Spare Parts**, contains a complete listing of the available spare parts and exploded views.

6.3 DISASSEMBLY SEQUENCE FLOW CHARTS

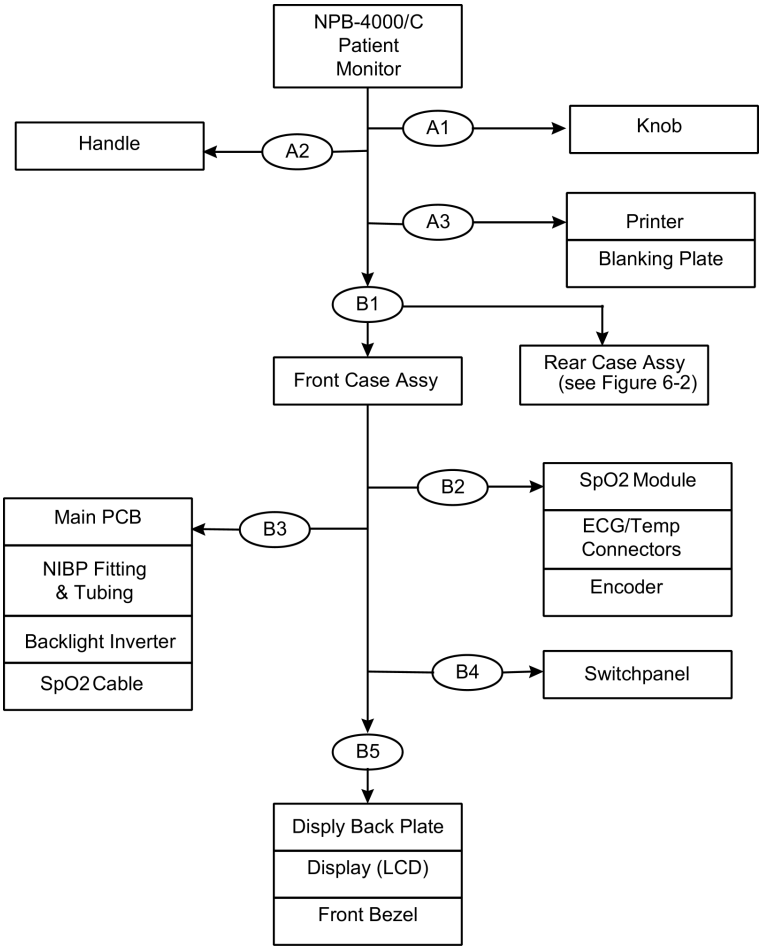


Figure 6-1: NPB-4000/C Disassembly Sequence Flow Chart, Sheet 1

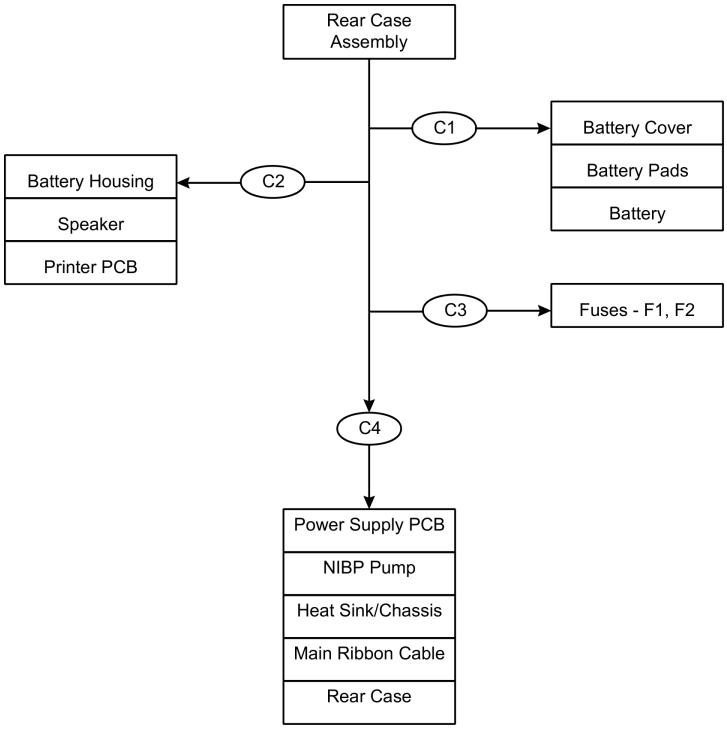


Figure 6-2: NPB-4000/C Disassembly Sequence Flow Chart, Sheet 2

6.4 CLOSED CASE DISASSEMBLY PROCEDURES

This section describes the items that may be removed/replaced without disassembling the main case of the monitor.

Step A1
Procedure
To remove front panel knob:
a) Knob is friction-fit on encoder shaft. Grasp sides of knob firmly and pull straight back from monitor; knob should slip off encoder shaft.
b) If knob does not move, separate front and rear cases as described in step B1. There is a hole in front cover behind knob; insert small screwdriver blade in hole and push firmly against back of knob.

Step A2

Procedure

To remove carrying handle:

a) Use screwdriver to remove two fastening screws and washers. Retain for reassembly.

b) Remove handle by sliding it straight back toward rear of monitor.

Illustration

Step A3

Procedure

To remove printer:

a) Press Paper Eject button on printer (right side). Door will drop forward.

b) Remove paper roll, if installed. Two fastening screws are visible at back panel of printer.

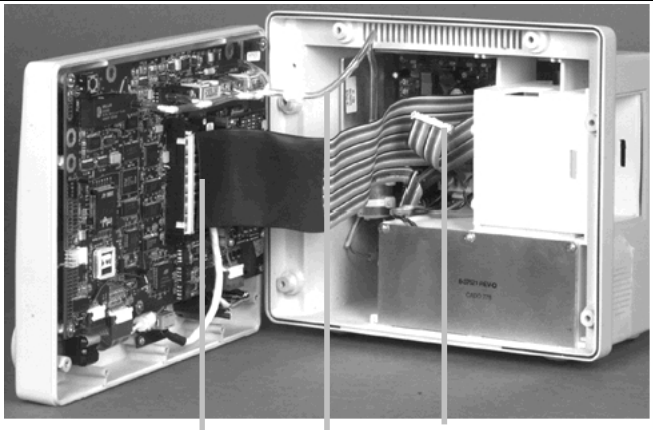
c) Use screwdriver to back out captive fastening screws.

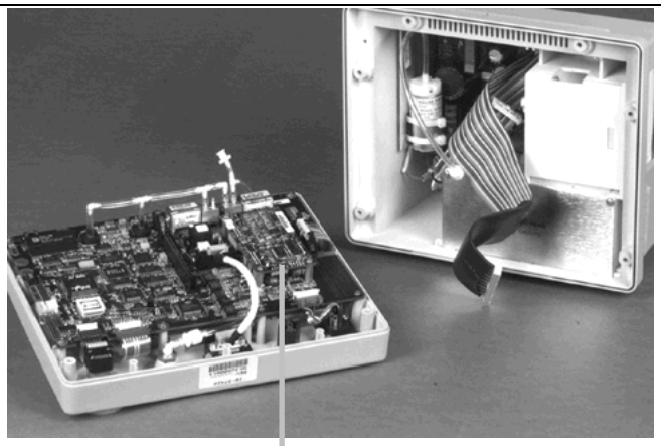
d) Pull printer straight out side of monitor, disengaging connector at rear of module from Printer PCB in assembly.

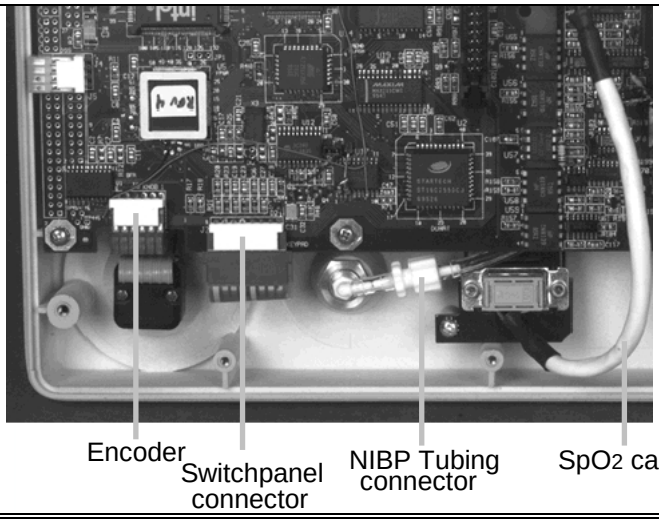
Removal of Printer PCB can be accomplished only after front and rear cases are separated.

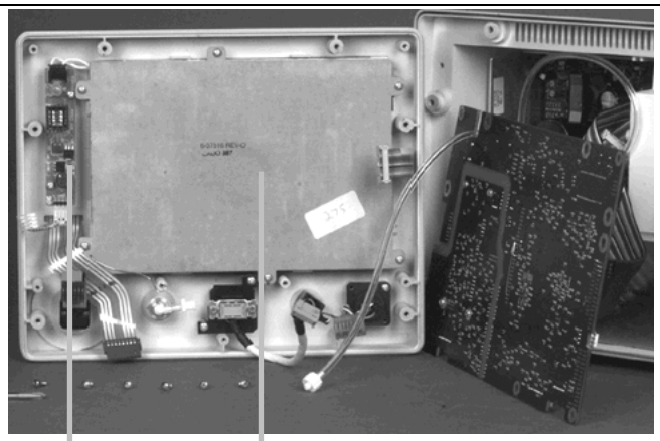
6.5 FRONT CASE DISASSEMBLY PROCEDURES

This section describes the steps to separate the front and rear case assemblies, and the items that may be removed/replaced on the front case assembly.

Step B1
Procedure
To separate front and rear case assemblies*:* a) Remove handle as indicated in step A1. b) Use screwdriver to remove four screws fastening Rear Case Assembly to Front Case Assembly. Retain for reassembly.
Illustration
Procedure
c) Separate two major case assemblies. There is enough cable and tubing slack to permit the two assemblies to remain at approximately a 90-degree angle to each other.
Illustration
 Main ribbon cable assembly NIBP tubing Connector to printer PCB (when installed)

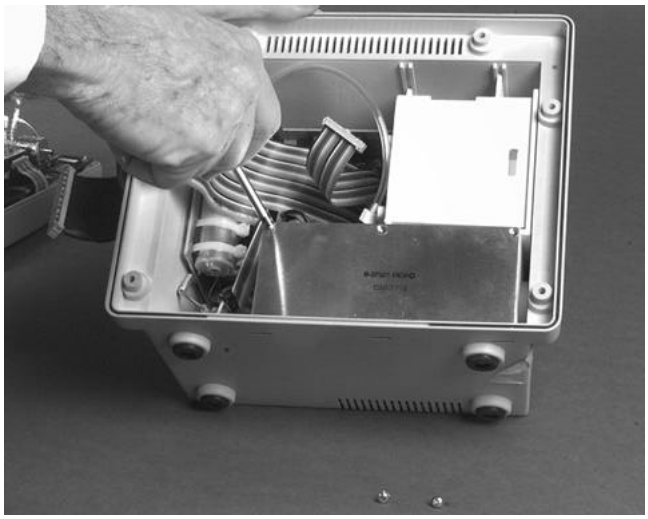
Procedure
d) Disconnect large ribbon-cable connector from main PCB.
e) Unscrew NIBP tubing connector from pump to main PCB. Front and rear case assemblies are now completely separable from one another.
Illustration
 SpO2 module
Step B2
Procedure
***To remove SpO2 module, ECG/Temp connector assembly, and encoder assembly**:*
• **SpO2 module**: remove three screws located at corners of SpO2 module, lift off ground wire and foil shield, pull SpO2 module straight up to disengage it from main PCB.
• **ECG/Temp cable/connector assembly:** unplug connector from Main PCB, remove screws fastening ECG connector to front case, rotate temperature connector counter-clockwise to unscrew it from fastening nut on outside of front case.
• **The encoder assembly:** unplug connector from main PCB. Remove knob, as described in step A1. Use 9/16" hex socket to unscrew fastening nut on outside of front case. Encoder may be pulled away from front case.

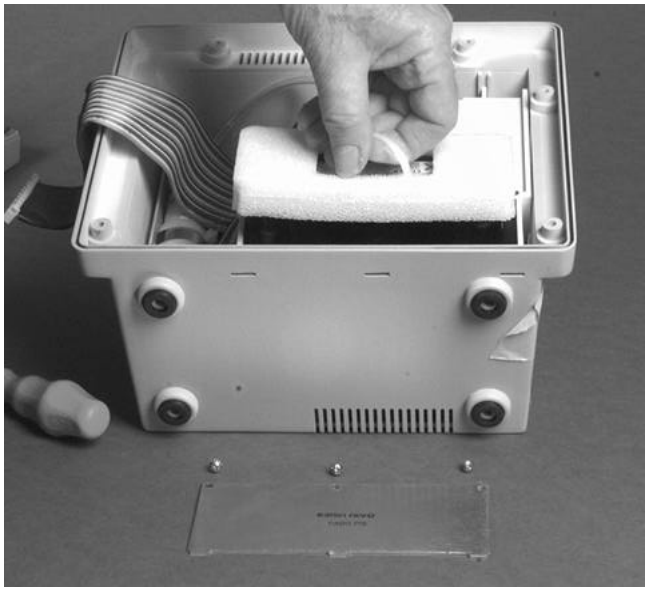
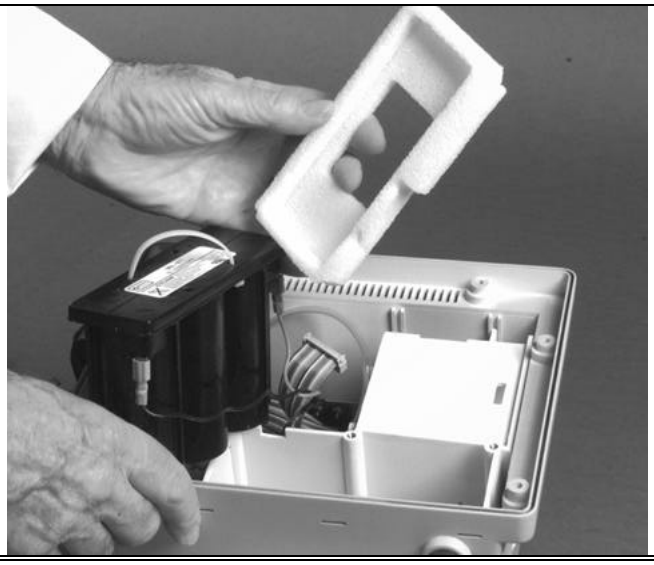
Step B3
Procedure
To remove main PCB: a) Disconnect connectors, from main PCB, for: • Switch panel • SpO_2 • ECG/Temp • Encoder • LCD (display) • Backlight
Illustration


Procedure
b) Use screwdriver to remove six fastening screws around periphery of main PCB. Retain fastening screws for reassembly. c) Lift main PCB slightly and unscrew tubing connector near NIBP front panel fitting. d) Main PCB may now be removed. This allows access to SpO_2 front panel connector, NIBP fitting and backlight inverter.
Illustration
 Backlight inverter Display back plate
Step B4
Procedure
To remove switch panel: a) Switch panel is attached with an adhesive to front panel. b) Carefully lift up one corner of switch panel, and peel switch panel away from front panel. When switch panel is free, feed connector through slot in front panel.
Step B5
Procedure
To remove LCD: a) Remove six fastening screws around periphery of display back plate. Retain fastening screws for reassembly. b) Carefully remove grounding straps, noting their location and orientation. Display back plate may now be removed. c) Disconnect backlight connector from backlight inverter. LCD may now be lifted out of front bezel assembly.

6.6 REAR CASE DISASSEMBLY PROCEDURES

This section describes the items that may be removed/replaced on the rear case assembly. First perform the procedure described in step B1 to separate the front and rear case assemblies.

Step C1
Procedure
To remove battery: a) Use screwdriver to remove three screws holding battery cover plate in place.
Illustration


Procedure
b) Grasp strap, accessible through opening in top foam cover, and gently pull battery from its housing.
Illustration

Procedure
c) Remove wire connectors from battery clips. Remember red wire is connected to plus (+) side of battery pack.
Illustration


Step C2

Procedure

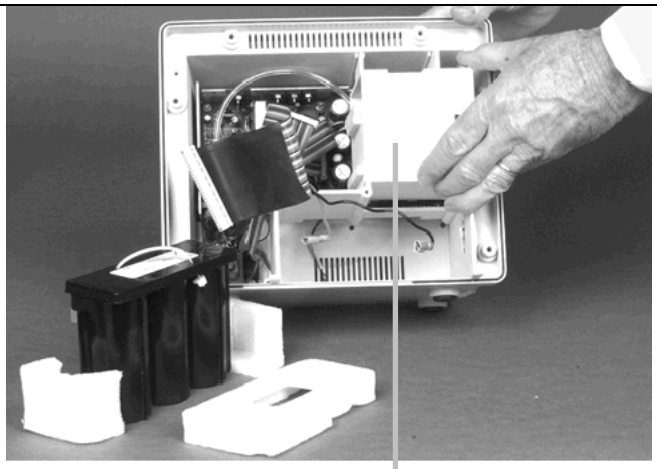
To remove battery housing:

a) Remove battery as described in step C1. Carefully remove two foam battery pads from battery housing.

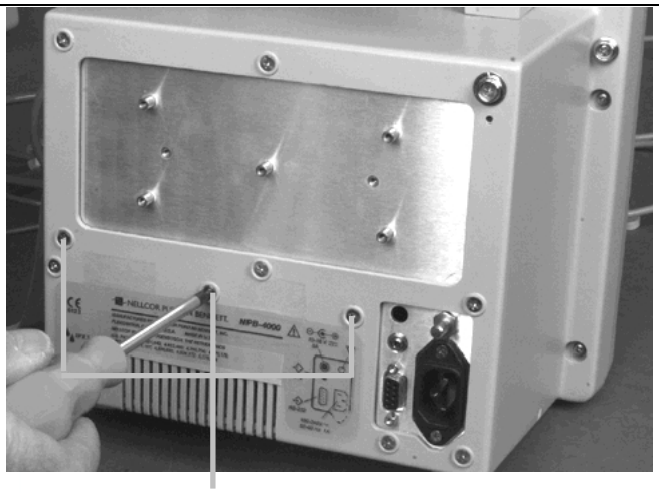
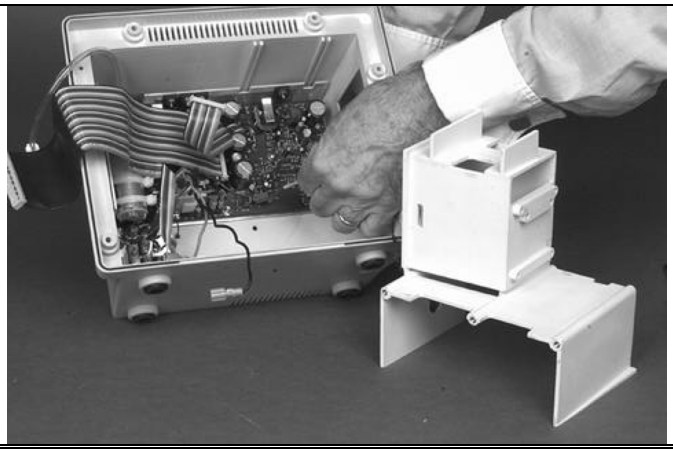
b) If a printer is installed, remove it as described in step A3.

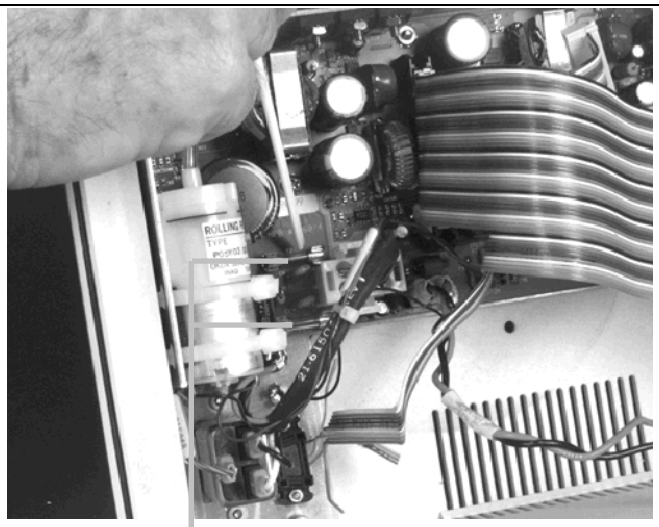
c) If a printer is not installed, remove printer blanking cover by slipping small flat-blade screwdriver into one of the slots on the blanking cover. Use screwdriver to gently depress snap-tab on inside of cover, while pulling cover away from monitor. After first tab is released, repeat process on other side of cover and remove cover.

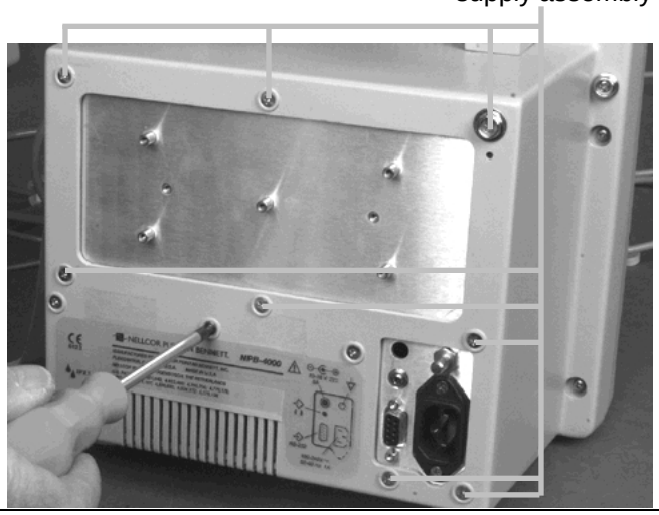
Illustration

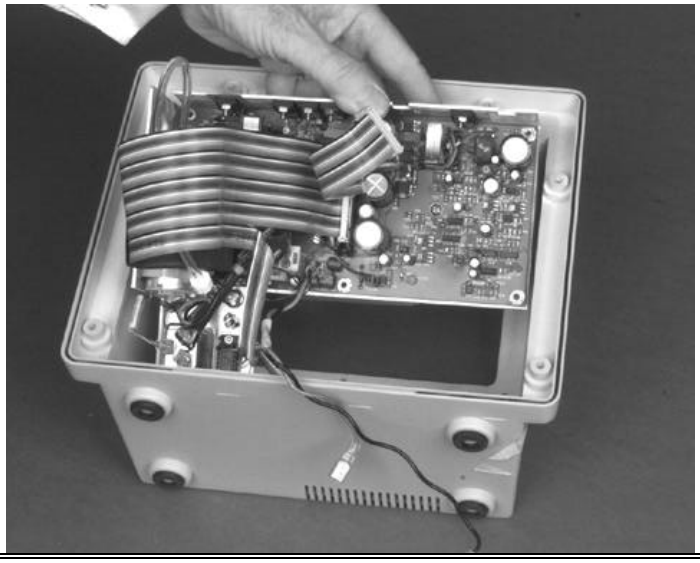


Battery housing

Procedure
d) On rear panel of monitor, remove three screws fastening battery housing. e) Carefully slide battery housing from rear case assembly.
Illustration
 Screws fastening battery housing
Procedure
f) Disconnect speaker twisted-pair-connector from power supply PCB. Speaker is mounted on one side of battery housing. g) If printer had been installed, disconnect ribbon cable from printer PCB. Printer PCB may be removed by removing four screws fastening PCB to battery housing.
Illustration


Step C3
Procedure
To remove fuses: a) Remove AC power input fuses, as shown, using fuse pullers.
Illustration
   Fuse F1 and F2

Step C4
Procedure
To remove power supply assembly*:*   *a)* On rear panel of monitor, remove eight screws fastening power supply assembly.
Illustration
Screws fastening power supply assembly   

Procedure
b) Carefully lift power supply assembly from rear case. c) Power supply assembly may be disassembled into the following elements: • Power supply PCB • NIBP pump • Heat sink/chassis • Main ribbon cable
Illustration


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7. SPARE PARTS

7.1 INTRODUCTION

Spare parts, along with part numbers, are shown in Table 7-1 through Table 7-7. "Item No." corresponds to the circled callout numbers in Figure 7-1 through Figure 7-6. The "Step Ref." corresponds to the disassembly steps described in Section 6.

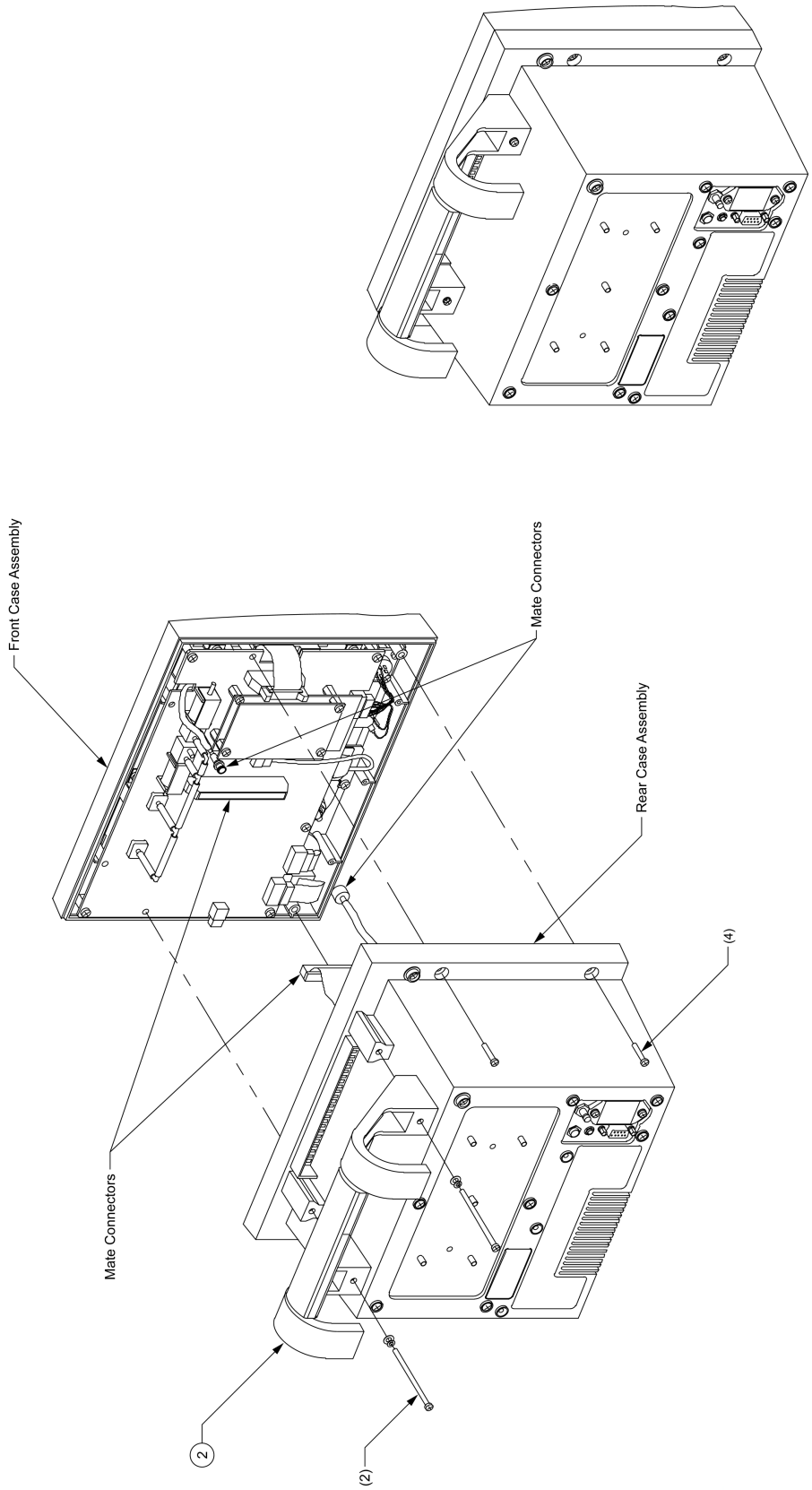

Figure 7-1: NPB-4000/C Top Assembly Drawing

Table 7-1: Top Assembly (Figure 7-1)

Item No.	Description	NPB Part No.	Step Ref.
NPB-4000			
2	Handle	047394	A2
NPB-4000C			
2	Handle	047394	A2

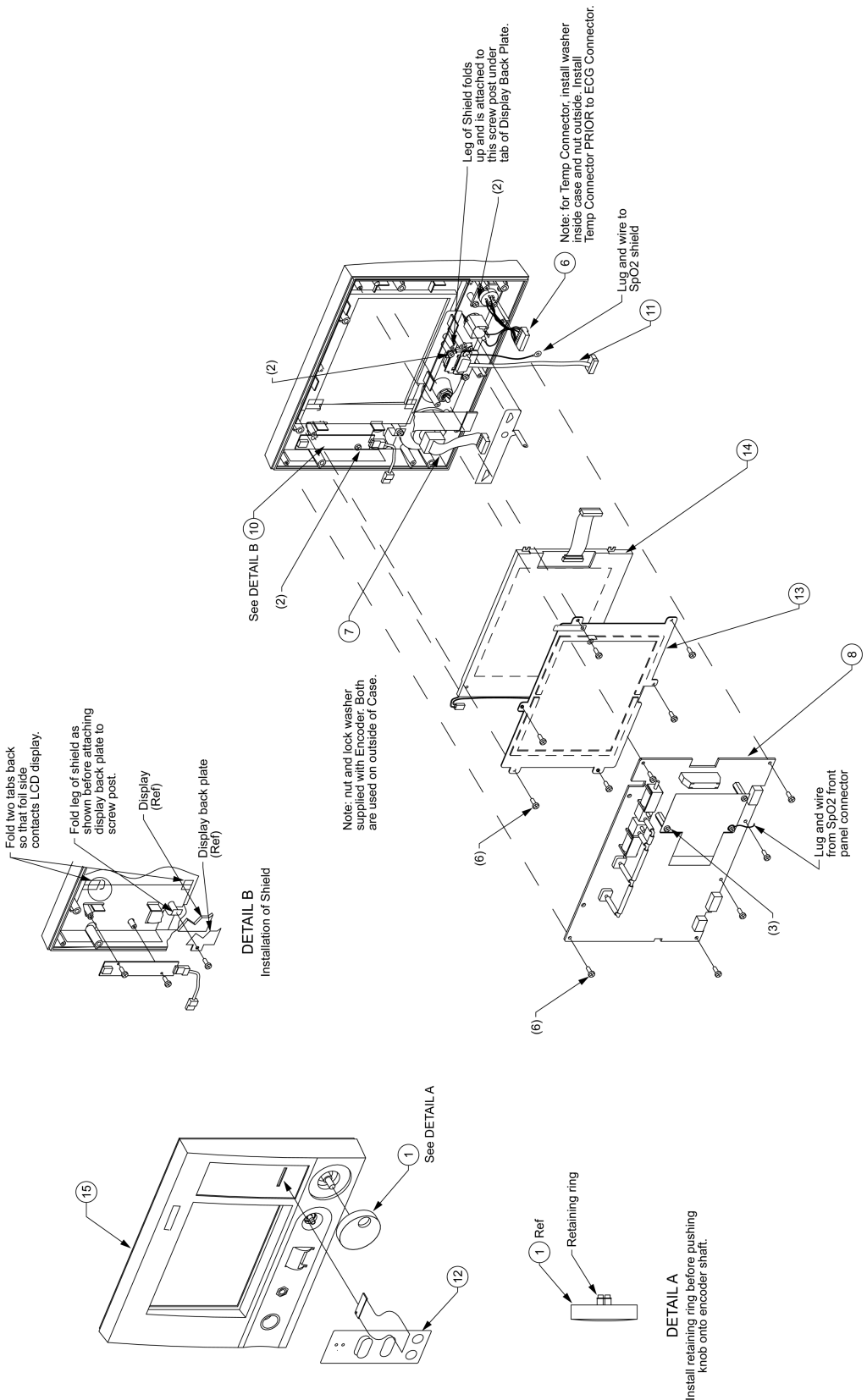
Leg of Shield folds up and is attached to this screw post under tab of Display Back Plate.
(2)
Note: for Temp Connector, install washer inside case and nut outside. Install Temp Connector PRIOR to ECG Connector.
6
Lug and wire to SpO2 shield
11
(2)
See DETAIL B
10
(2)
7
14
13
8
Note: nut and lock washer supplied with Encoder. Both are used on outside of Case.
(6)
Lug and wire from SpO2 front panel connector
(3)
(6)
Fold two tabs back so that foil side contacts LCD display.
Fold leg of shield as shown before attaching display back plate to screw post.
Display (Ref)
Display back plate (Ref)
DETAIL B
Installation of Shield
15
1
See DETAIL A
12
1
Ref
Retaining ring
DETAIL A
Install retaining ring before pushing knob onto encoder shaft.

Figure 7-2: NPB-4000/C Front Case Assembly Diagram (Sheet 1 of 2)

Table 7-2: Front Case Assembly (Figure 7-2)

Item No.	Description	NPB Part No.	Step Ref.
NPB-4000			
1	Knob	044727	A1
5	SpO_2 module	046085	B2
6	Connector/cable, ECG/temp	047376	B2
7	Encoder	291186	B2
8	PCB, main, Version 3.0	049624	B3
9	NIBP fitting and tubing	047375	B3
10	Inverter, backlight	047378	B3
11	Cable, SpO_2	060230	B3
12	Switch panel	046787	B4
13	Plate, display back	047379	B5
14	Display (LCD)	047377	B5
15	Bezel ,front	049623	B5
NPB-4000C			
1	Knob	044727	A1
5	SpO_2 module	046085	B2
6	Connector/cable, ECG/temp	047376	B2
7	Encoder	291186	B2
8	PCB, main	049591	B3
9	NIBP fitting and tubing	047375	B3
10	Inverter, backlight	049621	B3
11	Cable, SpO_2	060230	B3
12	Switch panel	046787	B4
13	Plate, display back	049592	B5
14	Display (LCD)	049593	B5
15	Bezel ,front	049589	B5

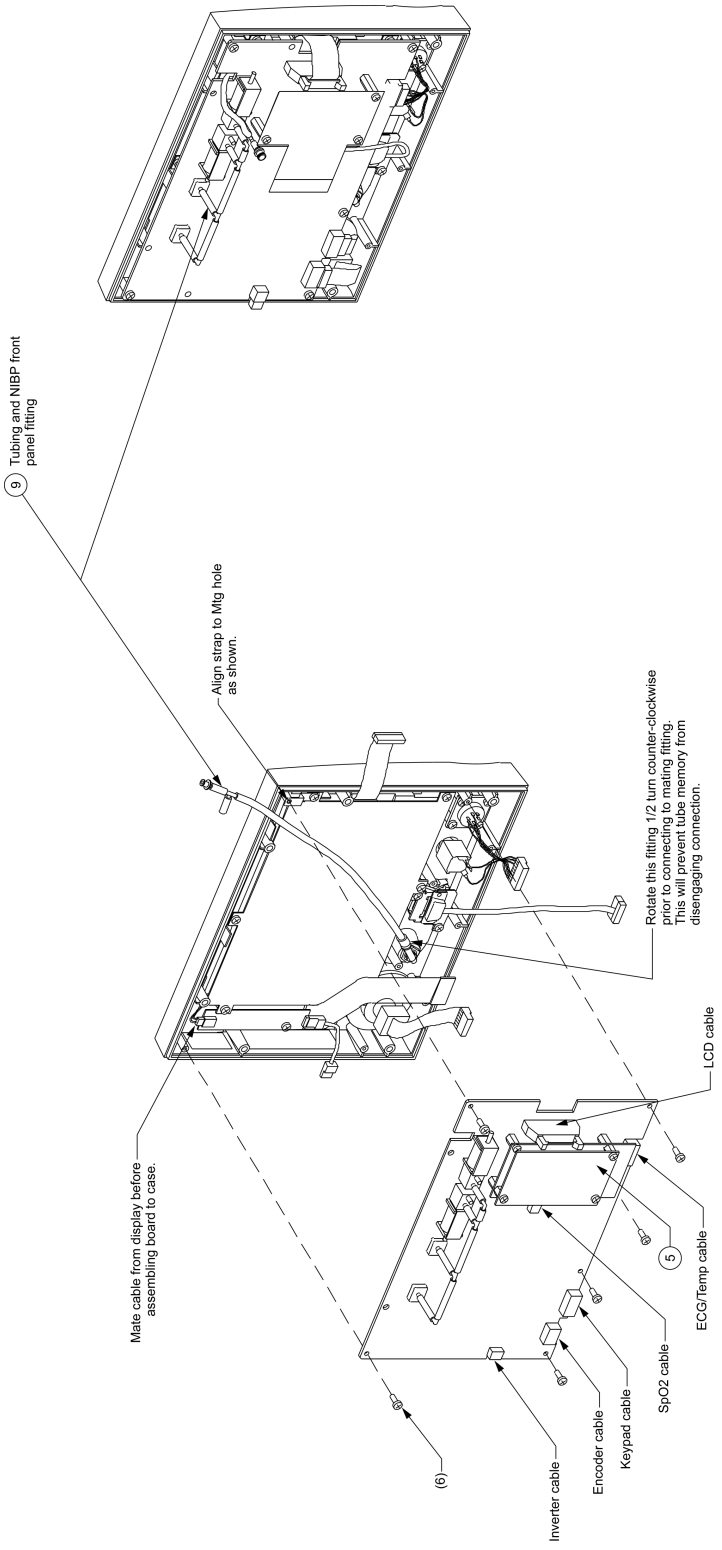
9 Tubing and NIBP front panel fitting
Align strap to Mtg hole as shown.
Rotate this fitting 1/2 turn counter-clockwise prior to connecting to mating fitting. This will prevent tube memory from disengaging connection.
LCD cable
Mate cable from display before assembling board to case.
5
ECG/Temp cable
SpO2 cable
Keypad cable
Encoder cable
Inverter cable
(6)

Figure 7-3: NPB-4000/C Front Case Assembly Diagram (Sheet 2 of 2)

Table 7-3: Front Case Assembly (Figure 7-3)

Item No.	Description	NPB Part No.	Step Ref.
NPB-4000			
1	Knob	044727	A1
5	SpO_2 module	046085	B2
6	Connector/cable, ECG/temp	047376	B2
7	Encoder	291186	B2
8	PCB, main	046073	B3
9	NIBP fitting and tubing	047375	B3
10	Inverter, backlight	047378	B3
11	Cable, SpO_2	045278	B3
12	Switch panel	046787	B4
13	Plate, display back	047379	B5
14	Display (LCD)	047377	B5
15	Bezel ,front	049589	B5
NPB-4000C			
1	Knob	044727	A1
5	SpO_2 module	046085	B2
6	Connector/cable, ECG/temp	047376	B2
7	Encoder	291186	B2
8	PCB, main	049591	B3
9	NIBP fitting and tubing	047375	B3
10	Inverter, backlight	047378	B3
11	Cable, SpO_2	060230	B3
12	Switch panel	046787	B4
13	Plate, display back	049592	B5
14	Display (LCD)	049593	B5
15	Bezel ,front	049589	B5

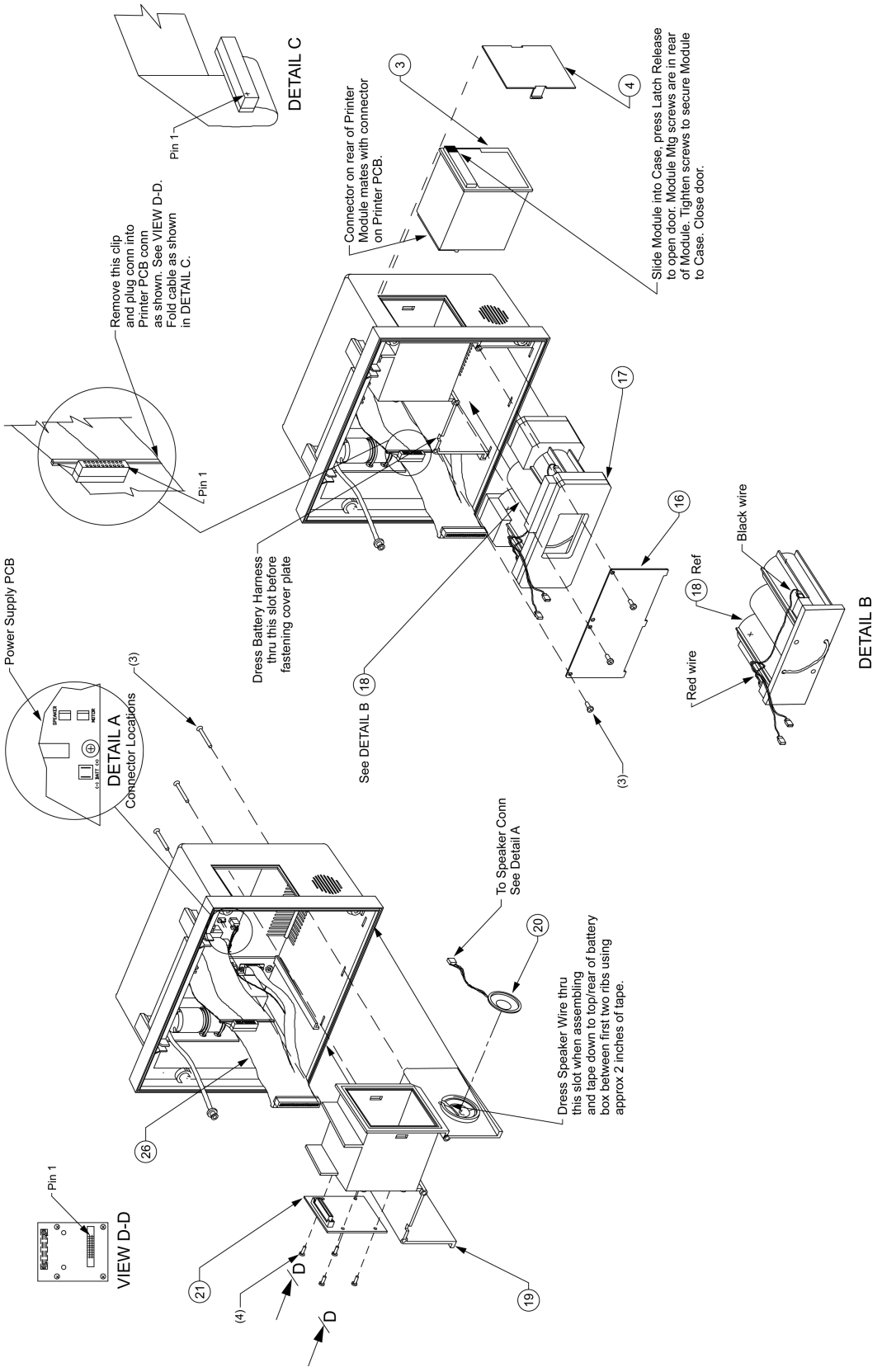
DETAIL C
Pin 1
Connector on rear of Printer Module mates with connector on Printer PCB.
Slide Module into Case, press Latch Release to open door. Module Mtg screws are in rear of Module. Tighten screws to secure Module to Case. Close door.
Remove this clip and plug conn into Printer PCB conn as shown. See VIEW D-D. Fold cable as shown in DETAIL C.
Pin 1
Dress Battery Harness thru this slot before fastening cover plate
See DETAIL B
Power Supply PCB
DETAIL A
Connector Locations
Black wire
Ref
Red wire
DETAIL B
To Speaker Conn See Detail A
Dress Speaker Wire thru this slot when assembling and tape down to top/rear of battery box between first two ribs using approx 2 inches of tape.
Pin 1
VIEW D-D
D
D

Figure 7-4: NPB-4000/C Rear Case Assembly Diagram (Sheet 1 of 2)

Table 7-4: Rear Case Assembly (Figure 7-4)

Item No.	Description	NPB Part No.	Step Ref.
NPB-4000			
3	Printer module	060480	A3
4	Plate, printer blanking	047386	A3
16	Cover, battery	047382	C1
17	Pads, battery	047383	C1
18	Battery	047384	C1
19	Housing, battery	047381	C2
20	Speaker	047387	C2
21	PCB, printer	047388	C2
26	Cable, main ribbon	047391	C4
27	Case, Rear	047393	C4
NPB-4000C			
3	Printer module	060480	A3
4	Plate, printer blanking	047386	A3
16	Cover, battery	047382	C1
17	Pads, battery	047383	C1
18	Battery	047384	C1
19	Housing, battery	047381	C2
20	Speaker	047387	C2
21	PCB, printer	047388	C2
26	Cable, main ribbon	047391	C4
27	Case, Rear	047393	C4

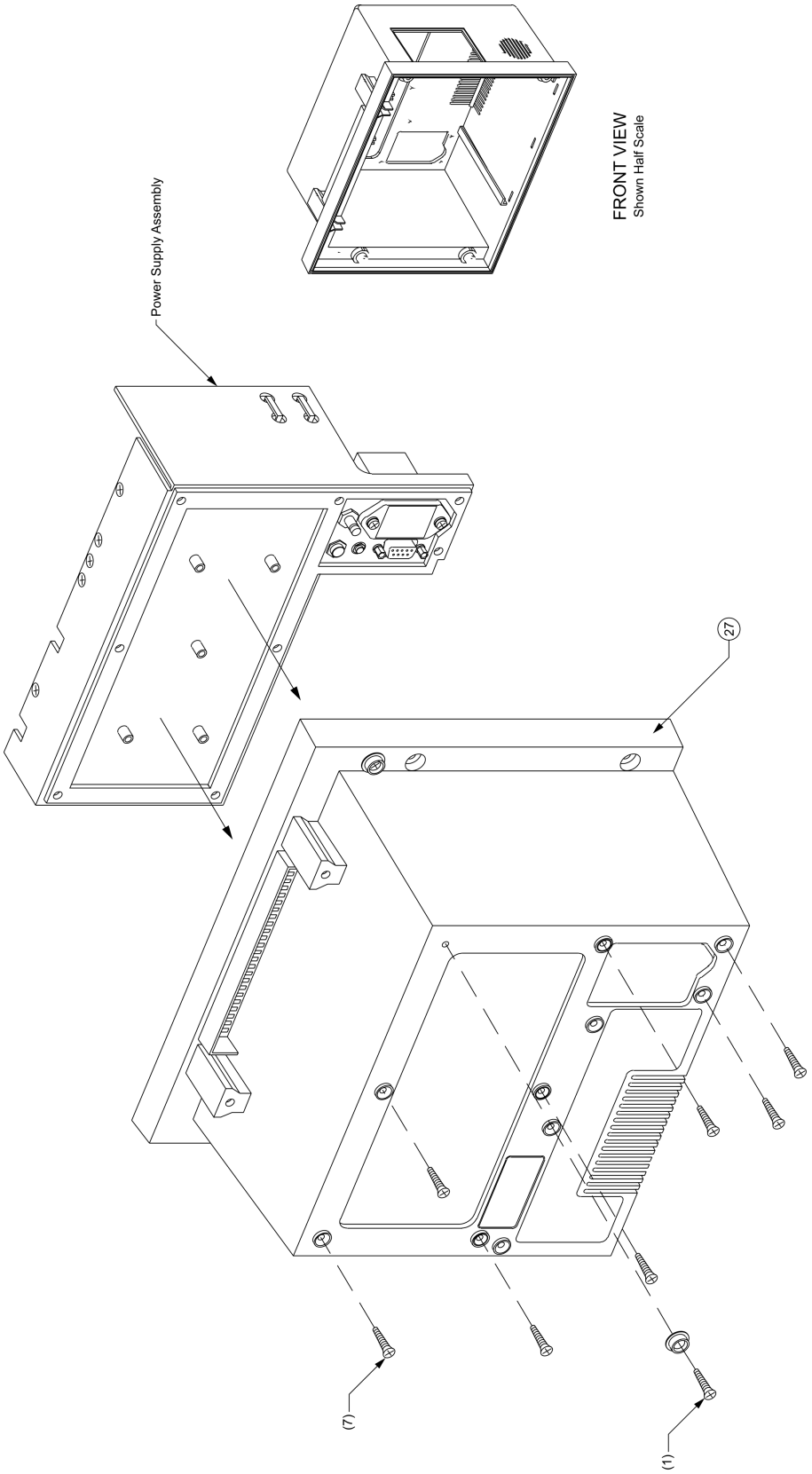

Figure 7-5: NPB-4000/C Rear Case Assembly Diagram (Sheet 2 of 2)

Table 7-5: Rear Case Assembly (Figure 7-5)

Item No.	Description	NPB Part No.	Step Ref.
NPB-4000			
3	Printer module	060480	A3
4	Plate, printer blanking	047386	A3
16	Cover, battery	047382	C1
17	Pads, battery	047383	C1
18	Battery	047384	C1
19	Housing, battery	047381	C2
20	Speaker	047387	C2
21	PCB, printer	047388	C2
26	Cable, main ribbon	047391	C4
27	Case, Rear	047393	C4
➡	Power Supply Assembly	049622	C6
NPB-4000C			
3	Printer module	060480	A3
4	Plate, printer blanking	047386	A3
16	Cover, battery	047382	C1
17	Pads, battery	047383	C1
18	Battery	047384	C1
19	Housing, battery	047381	C2
20	Speaker	047387	C2
21	PCB, printer	047388	C2
26	Cable, main ribbon	047391	C4
27	Case, Rear	047393	C4
➡	Power Supply Assembly	049622	C6

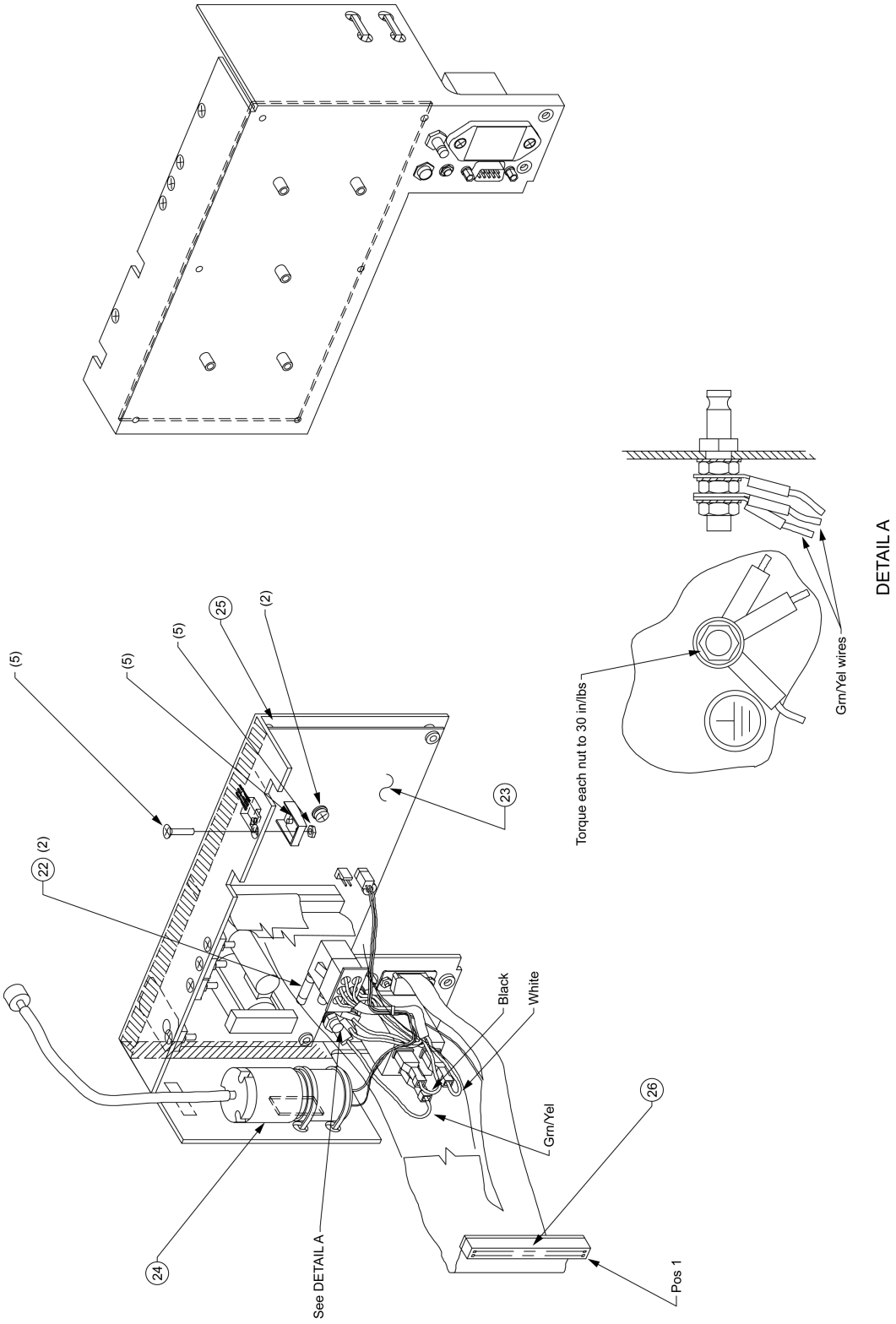

Figure 7-6: NPB-4000/C Power Supply/Heat Sink Assembly Diagram

Table 7-6: Power Supply Assembly (Figure 7-6)

Item No.	Description	NPB Part No.	Step Ref.
NPB-4000			
22	Fuse, 0.75A, slo-blow, 250V, 5x20 mm	691501	C3
23	PCB, power supply	046074	C4
24	Pump, NIBP	047389	C4
26	Cable, main ribbon	047391	C4
NPB-4000C			
22	Fuse, 0.75A, slo-blow, 250V, 5x20 mm	691501	C3
23	PCB, power supply	046074	C4
24	Pump, NIBP	047389	C4
26	Cable, main ribbon	047391	C4

Some of the accessories available for the NPB-4000/C are listed below.

Table 7-7: NPB-4000/C Accessories

NPB Part No.	Description
CE-10	ECG cable
LE-3SI	ECG leads (IEC color code)
LE-3SN	ECG leads (AHA color code)
ASP3	*Oxisensor® II* sensor assortment pack
DS100A	*Durasensor®* oxygen transducer
EC-8	SpO_2 sensor extension cable
SHBP-10	NIBP hose
902096	Printer paper (10 rolls)
045279	GCX mounting plate
046270	GCX roll stand
046283	GCX wall mount
045992	Accessory bag
044997	DC input cable
044998	Defib sync cable

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SECTION 8: PACKING FOR SHIPMENT

8.1 General Instructions
8.2 Repackaging in Original Carton
8.3 Repackaging in a Different Carton

8. PACKING FOR SHIPMENT

To ship the monitor for any reason, follow the instructions in this section.

8.1 GENERAL INSTRUCTIONS

Pack the monitor carefully. Failure to follow the instructions in this section may result in loss or damage not covered by the Mallinckrodt warranty. If the original shipping carton is not available, use another suitable carton; North American customers may call Mallinckrodt Technical Services to obtain a shipping carton.

Prior to shipping the monitor, contact your supplier or the local Mallinckrodt office (Technical Services Department) for a returned goods authorization (RGA) number. Mark the shipping carton and any shipping documents with the returned goods authorization number.

8.2 REPACKING IN ORIGINAL CARTON

If available, use the original carton and packing materials. Pack the monitor as follows:

1. Place the monitor and, if necessary, accessory items in original packaging.
2. Place in shipping carton and seal carton with packaging tape.
3. Label carton with shipping address, return address and RGA number, if applicable.

8.3 REPACKING IN A DIFFERENT CARTON

If the original carton is not available, use the following procedure to pack the NPB-4000/C:

1. Place the monitor in a plastic bag.
2. Locate a corrugated cardboard shipping carton with at least 200 pounds per square inch (psi) bursting strength.
3. Fill the bottom of the carton with at least 2 inches of packing material.
4. Place the bagged unit on the layer of packing material and fill the box completely with packing material.

5. Seal the carton with packing tape.

6. Label the carton with the shipping address, return address, and RGA number, if applicable.

SECTION 9: SPECIFICATIONS

9.1 Scope
9.2 General
9.3 Electrical
9.4 Environmental
9.5 Measuring Parameters
9.6 Trends

9. SPECIFICATIONS

9.1 SCOPE

This section includes specifications for the NPB-4000/C. The instrument is designed to monitor patient vital signs, including: electrocardiogram and heart rate, respiration rate, noninvasive blood pressure, blood oxygen saturation, and temperature. In addition to displaying the instantaneous values of the measured parameters, the NPB-4000/C includes provisions for displaying waveform data, as well as trends in graphical and tabular format. An optional printer provides for hard copy recording.

9.2 GENERAL

Size**:**	10.6 in. x 8.6 in. x 6.5 in. (26.9 cm x 21.8 cm x 16.5 cm) excluding handle
Weight:	10.8 lb. (4.9 kg) excluding accessories, options, cables
Display:	
NPB-4000	
Screen Type:	Liquid Crystal Display (LCD), Monochrome, Cold Cathode Fluorescent Backlit
Screen Size:	151 mm x 113 mm
Resolution:	640 x 480 pixel
NPB-4000C	
Screen Type:	Liquid Crystal Display (LCD) Color, Cold Cathode Fluorescent Backlit
Screen Size:	130 mm x 97 mm
Resolution:	640 x 480 pixel
Printer (optional):	
Type:	Thermal
Weight:	0.9 lb. (0.4 kg)
Paper Width:	50 mm
Speeds:	25 mm/s and 50 mm/s
Safety Standards:	IEC 601-1, UL 2601-1, Can/CSA C22.2 601.1-M90

Protection Class:	Class I, internally powered equipment: per IEC 601-1, clause 2.2.4
Degree of Protection:	Type CF: per IEC 601-1, clause 2.2.26
Mode of operation:	Continuous

9.3 ELECTRICAL

Internal Battery:	6V, 8 Ampere-Hours; Type - sealed lead-acid
Battery Operating Time:	
NPB-4000	4 hours typical @ 25˚C, no printing, one NIBP measurement per 15 min. (fully charged battery)
NPB-4000C	3 hours typical @ 25˚C, no printing, one NIBP measurement per 15 min. (fully charged battery)
AC Mains:	100 VAC to 240 VAC, 50 Hz to 60 Hz, 1A max
DC (External):	10 VDC to 16 VDC, 5A max

9.4 ENVIRONMENTAL

Mechanical Shock:	IEC 68-2-27 100g; 6 msec; three axes 18 total shocks, nonoperating
Mechanical Vibration:	
Sinusoidal:	IEC 68-2-6 10 Hz to 58 Hz; 0.15 in. displacement 58 Hz to 150 Hz; 2g acceleration 4 min/sweep; 20 sweeps/axis, nonoperating
Temperature:	
Operating:	0 º C to 50˚C
Storage:	-20 º C to 60˚C
Humidity:	
Operating:	5 % RH to 95% RH, noncondensing
Storage:	5 % RH to 95% RH, noncondensing
Water Resistance:	IEC 529 Classification IPX1 (Protected against vertically dripping water)
Altitude:	0 ft to10,000 ft (operating)
	(1037 hPa to 697 hPa)
Electromagnetic Compatibility:	Radiated and conducted electromagnetic energy per CISPR 11, Class B

9.5 MEASURING PARAMETERS

9.5.1 ECG Measurement/Display

Heart Rate Range:	20 BPM - 250 BPM
Heart Rate Accuracy:	±5 BPM
Bandwidth:	
Normal Monitoring:	0.5 Hz to 40 Hz
Extended Low Frequency Response:	0.05 Hz to 40 Hz
Leads:	3 Lead (user selectable)
Display Sweep Speeds:	12.5 mm/sec, 25 mm/sec, and 50 mm/sec
Pacemaker Detection:	Indicator on waveform display, user selectable
ECG Size (sensitivity):	0.5 mV/cm, 1 mV/cm, 2 mV/cm, 4 mV/cm
Lead Off Detection:	Detected and displayed
Input Impedance:	> 5 MΩ
CMMR (common mode rejection ratio):	> 90 dB at 50 Hz or 60 Hz
Input Dynamic Range:	±5 mV AC, ±300 mV DC
Defibrillator Discharge:	<5 sec per IEC 601-2-27
Recovery:	<8 sec per AAMI EC13-1992

Standards: Meets the performance standards of ANSI/AAMI EC13-1992. Instead of a 1 mV standardizing voltage *(section 3.2.2.9),* a fixed, 1 cm reference bar is always present in the ECG display, along with the ECG size setting expressed in mV/cm. The following information references particular sections of ANSI/AAMI EC13-1992.	
Respiration, leads-off sensing waveform. *3.1.2.1(b)*	A 100 kHz square wave is used to inject 42 mA, p-p differentially between RA and LA.
Tall T-wave rejection. *3.1.2.1(c)*	T-wave of 0.8 mV amplitude will not affect heart rate determination.
Heart rate averaging. *3.1.2.1(d)*	Averages six of the most recent eight detected R-R intervals excluding the longest and shortest of the eight intervals.

Response to irregular rhythm. *3.1.2.1(e)*	a) Ventricular bigeminy - 80 BPM b) Slow alternating ventricular bigeminy - 60 BPM c) Rapid alternating ventricular bigeminy - 120 BPM d) Bi-directional systoles - 89 to 96 BPM	
Heart rate meter response time. *3.1.2.1(f)*	a) Change from 80 to 120 BPM: 4 to 6 sec b) Change from 80 to 40 BPM: 6 to 7 sec	
Time to alarm for tachycardia. *3.1.2.1(g)*	<u>Waveform 4(a) Amplitude</u> 0.5 mV 1 mV 2 mV <u>Waveform 4(b) Amplitude</u> 1 mV 2 mV 4 mV	<u>Avg. Time to Alarm</u> 4 sec 4 sec 4 sec <u>Avg. Time to Alarm</u> 3 sec 3 sec 3 sec
Pacemaker pulse rejection. *3.1.4.1, 3.1.4.2*	With the exceptions noted below, the monitor will reject all pacemaker pulses having amplitudes of ±2 to ±700 mV and pulse widths from 0.1 to 2 ms, with and without under/overshoot. Following are pacer pulse conditions that the monitor will reject, but are less than the maximum range listed in the standard:	
	Pacer pulse width = 2 ms, double pulse, without over/undershoot, no QRS	Pacer amplitude = ±300 mV
	Pacer pulse width = 2 ms, single and double pulse, with 2 mV over/undershoot, no QRS	Pacer amplitude = ±300 mV
	Pacer pulse width = 0.1 ms, double pulse, with 2 mV over/undershoot, ineffective pacing	Pacer amplitude = +300 mV, -450 mV

9.5.2 Respiration Measurement/Display

Technique:	Trans-thoracic impedance
Range:	3 breaths/min to 150 breaths/min
Accuracy:	±3 breaths/min
Leads:	RA to LA
Display Sweep Speeds:	6.25 mm/s, 12.5 mm/s, 25 mm/s
Lead Off Condition:	Detected and displayed

9.5.3 NIBP (Noninvasive Blood Pressure) Measurement/Display

Note: Systolic and diastolic blood pressure measurements determined with this device are equivalent to those obtained by a trained observer using the cuff/stethoscope auscultation method, within the limits prescribed by the American National Standard, *Electronic or automated sphygmomanometers.*

Technique:	Oscillometric
Measurement Modes:	
Auto:	Automatic BP measurements at intervals of 1, 3, 5, 10, 15, 30, 60, and 90 minutes
Manual:	Single measurement initiated by NIBP Start/Stop switch
STAT:	Series of consecutive measurements for 5 minutes
Cuff Pressure Display:	10mmHg to 300 mmHg
Blood Pressure Measurement Range:	
Systolic:	60 mmHg to 250 mmHg
Mean Arterial Pressure:	30 mmHg to 235 mmHg
Diastolic:	20 mmHg to 220 mmHg
Pulse Rate Range:	20 BPM to 200 BPM
Blood Pressure Accuracy:	Mean error and standard deviation per ANSI/AAMI SP10, 1992
Pulse Rate Accuracy:	Greater of ±2 BPM or ±2% of pulse rate value
Initial Cuff Inflation:	180 mmHg (factory default), selectable 100 mmHg to 280 mmHg, in 20 mmHg intervals
Subsequent Cuff Inflation:	Previous SYS + 50 mmHg
Standards:	Meets performance standards of ANSI/AAMI SP10-1992

9.5.4 Temperature Measurement/Display

Technique:	Thermistor probe (YSI 400 series compatible)
Range:	15° C to 45° C
Accuracy:	±0.1° C

9.5.5 SpO_2 Measurement/Display

Range:

Pulse Rate:	20 BPM to 250 BPM
% Saturation:	0 % to 100%

Accuracy:

Pulse Rate:	±3 BPM
SpO_2:	70 % to 100%: ±2 digits 0 % to 69%: Unspecified

SpO_2 accuracies are expressed as plus or minus "X" digits (saturation percentage points) between saturations of 70–100%. This variation equals plus or minus one standard deviation (1SD), which encompasses 68% of the population. All accuracy specifications are based on testing the subject monitor on healthy adult volunteers in induced hypoxia studies across the specified range. Adult accuracy is determined with *Oxisensor® II* D-25 sensors.

9.6 TRENDS

Types:	Graphical and Tabular
Memory Storage:	12 hours, nonvolatile
Data interval:	20 seconds: (Stored data point is the average over 20-second interval)
Graphical Format:	One graph per vital sign
Display range:	2 hours, scrollable
Vertical Scaling:	
Heart rate:	50 BPM to 100 BPM, 0 BPM to 250 BPM, 25 BPM to 125 BPM
NIBP:	50 mmHg to 100 mmHg, 0 mmHg to 150 mmHg, 0 mmHg to 300 mmHg
SpO_2:	0% to 100%, 60% to 100%, 80% to 100 %
Respiration Rate:	0 BPM to 20 BPM, 0 BPM to 50 BPM, 0 BPM to 150 BPM
Temperature °C:	15º C to 45º C, 33º C to 41º C, 35º C to 39 ° C
Temperature °F:	55º F to 155º F, 91º to 107º F, 96º F to 102° F
Tabular Format:	One table for all variables Six fields per row (time and 5 vital signs)
Display interval:	Per NIBP measurement, or 15 minutes for no NIBP, or 20 seconds during alarm condition.

SECTION 10: INTRODUCTION AND SYSTEM DESCRIPTION

10.1 System Overview
10.2 System Block Diagram
10.3 ECG Processing
10.4 Respiration Processing
10.5 NIBP Processing
10.6 SpO_2 Processing
10.7 Temperature Processing

10. INTRODUCTION AND SYSTEM DESCRIPTION

10.1 SYSTEM OVERVIEW

10.1.1 The Complete NPB-4000/C Patient Monitor System

The NPB-4000/C patient monitor is a full-function monitor for use on adult and pediatric patients. The functions performed by the system include monitoring patient ECG, heart rate, respiration rate, blood pressures, blood oxygen saturation, and temperature.

In addition to monitoring and displaying the status of these physiological parameters, the instrument performs various microprocessor-programmed analytical functions, such as:

- Creating both visual and audible alarm signals when settable limits are violated;
- Creating and displaying warning messages when conditions are detected that would degrade or prevent valid measurements;
- Creating and displaying trend waveforms or tabular data;
- Providing a synchronizing pulse for defibrillator operation;
- Providing input to an optional recorder for printout of current or trend waveforms or tabular data.

The monitor is essentially a battery-powered instrument. An internal charging unit is designed to accept either an AC line voltage or DC source input voltage. The charger uses these external power sources to maintain a "float" voltage source available from the batteries.

10.2 SYSTEM BLOCK DIAGRAM

The NPB-4000/C patient monitor functions are represented graphically in the System Block Diagram, Figure 10-1.

Each section of the System Block Diagram is described briefly in the text that follows the illustration. This is followed by more detailed descriptions of the theory of operation of each block.

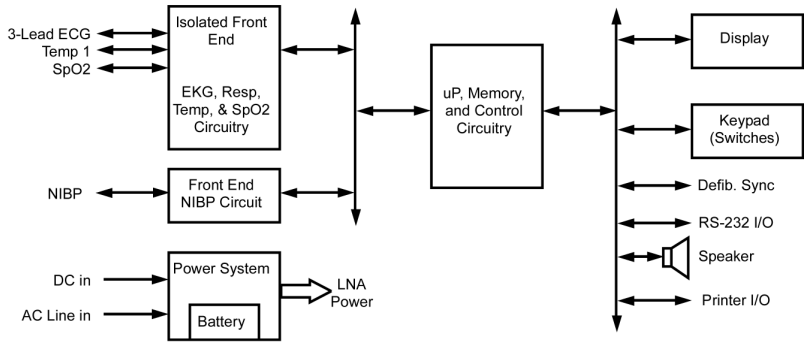

Figure 10-1: NPB-4000/C System Block Diagram

10.2.1 Isolated Front End

The Isolated Front End section includes all the circuitry to convert ECG, SpO_2, and temperature measurements to digital format and to connect this information to the processor. The respiration detection is obtained from two of the three electrodes of the ECG connections.

Galvanic isolation of these circuits from the remainder of the monitor is accomplished by utilizing an isolated power supply and by incorporating opto-isolators between the Front End outputs and inputs to the microprocessor computation and control circuitry.

10.2.2 NIBP Front End

The NIBP section contains the pumps, valves, pressure measurement circuitry, and control circuitry for the noninvasive blood pressure measurement. Pressure data is converted to digital format and conveyed to the processor section.

10.2.3 Power System

The power system section contains a power supply capable of operating the monitor and charging the battery from either an AC source of 100 to 240 volts AC at 50 to 60 Hz or a 10 to 16 volt DC input. This section also contains the battery, battery monitoring circuitry, and battery charging circuitry. The battery provides the operating power for the monitor.

Power system outputs of ±12 volts DC, +5 volts DC, and -24 volts DC are developed for use throughout the non-isolated portions of the monitor.

10.2.4 µP, Memory, and Control

The microprocessor (µP), Memory, and Control section contains the system CPU and all digital support circuitry. The latter includes the RAM, nonvolatile memory, and real-time clock. This section also contains the display logic, keypad (switch) interface logic, RS-232 I/O control, defibrillator synchronization control, and printer logic.

10.2.5 Display

The display is a cold-cathode, backlighted, fluorescent LCD unit. The pixel resolution of 0.23 mm provides a 640x480 line display. The NPB-4000 display is presented in black and white mode only (no gray scale). The NPB-4000C display is presented in color.

10.2.6 Keypad (Switches) and Knob

The keypad circuit contains five push-switch membrane switches and two green LEDs. The LEDs are driven by the power supply system and indicate the source of externally applied power mains (AC or DC), the charging of the batteries, and the condition of the source cable in-line fuses. Signals from the LEDs are returned to the microcomputer for processing and control as required.

The **power switch**, connected directly to the supply, toggles the power between Standby and On modes. When in Standby, the display is blank, and no monitoring is performed. However, the batteries are charging if either an AC or DC power source is connected to the rear panel.

The **alarm silencing switch** is connected directly to the processor and to the system power supply. Pressing this switch turns off the battery fuse alarm in the system power supply. Response of the processor depends upon the action in pressing this switch. If momentarily pressed (less than 2 seconds), alarms are silenced temporarily for a preset interval determined by the menu selection. If held pressed for 2 seconds or more, the Alarm Suspend condition is initiated.

The **NIBP switch** output is connected to the processor. Response of the processor depends upon the state of NIBP operation at the time and the action in pressing this switch. If momentarily pressed (less than 2 seconds), a single NIBP measurement is obtained. If pressed for 2 seconds or more, the processor initiates a STAT monitoring sequence. Pressing the NIBP switch at any time a pressure measurement is in effect will cause the processor to terminate the measurement and to deflate the cuff.

NPB-4000. The display **Contrast switch**, operates in conjunction with the Nellcor knob to determine the apparent black/white contrast setting in the display. Changing contrast is actually a change in the viewing angle. Outputs of the switch and knob are connected to the processor. Momentary pressing the switch sets the contrast to mid-range, factory-default value. Momentary pressing the switch, followed within 3 seconds by a rotation of the knob, are processed to vary the contrast of the display. When there has been no knob rotation for three seconds, the contrast control function is terminated by the processor. The contrast control function also is terminated if the knob is pressed any time within this 3-second interval.

NPB-4000C. Pressing the **Contrast switch** changes the background color from white to black or black to white.

Operation of the **Volume switch** accomplishes similar functions for the volume of the heart rate audible tone as the display contrast control switch does for the display. Pressing this switch enables the knob to vary the tone volume. The same timing consideration of 3 seconds is provided, in which to adjust the tone volume or to terminate the action.

10.2.7 Nellcor Knob

This is a rotating, push-switch knob. The associated knob circuitry generates a pulse when pressed and generates a digitally encoded pair of quadrature signals whose relative magnitudes and polarities represent the angular position of the knob. These outputs are connected to the processor where they are interpreted as required for the functions involved. Successive angular positions determine the direction of knob rotation.

In addition to the functions performed when in conjunction with the keypad switches as described above, the Knob operates in conjunction with the display to select menus and lists of parameter variables.

10.2.8 RS-232 I/O

This is a rear panel 9-pin connector providing interfaces with other computer systems or equipment. The driver for this "port" is a Universal Asynchronous Receive-Transmit (UART) integrated circuit that interfaces this port with the microprocessor. The baud rate for this serial transmission function is programmable from 1200 baud to 38.4 kilobaud.

One pin (9) of RS-232 connector is reserved for a **Nurse Call** signal. The Nurse call signal reacts when a low, medium, or high level alarm is activated.

10.2.9 Defib Synch Pulse

The rear-panel connector for the Defib Sync Pulse is keyed so that the connection of a cable can be detected by the processor. When a connection is detected, the processor software initiates the generation by hardware of a TTL-compatible pulse capable of driving 1 TTL load over a three-meter cable with less than 200 pF capacitance.

The defib pulse is triggered by the detection of the R-wave in the QRS sequence of the ECG waveform complex. The pulse signal is active for 100±10 milliseconds.

10.2.10 Speaker

The speaker is capable of providing 73 dBA of volume at a distance of one meter during alarm conditions. The processor drives the speaker in different patterns as specified for the different alarm priorities and conditions. Refer to the operator's manual for descriptions of alarm responses.

10.2.11 Recorder

The optional recorder (printer) module is installed in the right panel of the monitor. Refer to the NPB-4000/C monitor operator's manual for printing procedures. It provides users with the capability to obtain hard-copy records of selected vital signs information. Basic control of the recorder is implemented by two push-switch controls on the recorder front panel. One of these is used to obtain continuous recordings of the real-time waveforms displayed in the top two graphic frames. Along with the waveforms, the recorder prints the values of the vital signs being displayed. The printing continues until the user presses either recorder switch a second time.

The other control switch initiates a printout for 20 seconds of the same information recorded by the continuous control.

If scrolling is enabled in a display frame containing trend data when the continuous recording switch is operated, then the trend record for that vital sign is printed. If the snapshot recording switch is operated, then only the trend data on the display is printed.

The recorder may be programmed via the monitor menu display to print a snapshot recording when an alarm condition occurs.

Printing is accomplished on 50-mm wide thermal paper at printer speeds programmable up to 50 mm/sec.

10.3 ECG PROCESSING

The technique used in ECG senses the varying potential difference between two points at the skin surface which respond to the chemical actions of the muscular activity of the heart.

Three electrodes are attached to the patient's right arm (RA), left arm (LA) and left leg (LL). The varying potentials at these locations are cable-connected to the ECG circuit inputs where they are conditioned, and the difference of potential between two selected leads is digitized before transmitting through opto-isolators to the processor. The processor-installed algorithms operate on the signals to develop drivers for the graphic display and to compute the heart rate in beats per minute (bpm).

In addition to the acquisition of the QRS waveform complex, the ECG input and subsequent signal processing computing circuitry perform a number of other functions:

- They detect a "lead-off" condition if one of the electrode connections is disrupted.
- They detect the presence of pacemaker signals within the QRS waveform complex of the ECG.
- They generate a synchronization pulse for external use with defibrillators. The Defib Synch Pulse output is available at a connector in the rear panel.

10.4 RESPIRATION PROCESSING

The patient's respiration is detected by using two of the three leads of the ECG electrodes and cable. A low-level excitation signal is applied to these leads, and the variation of the thoracic impedance caused by the breathing is sensed and processed for display and measurement.

10.5 NIBP PROCESSING

The NIBP processing uses an oscillometric technique to provide needed measurements at selected intervals. This technique uses an inflatable sphygmomanometer cuff similar to those used by clinicians in routine measurements.

A motorized pump inflates the cuff to approximately 180 mmHg initially, at which point the pressure effectively stops the flow of blood. Then, under monitor control, the pressure in the cuff is gradually reduced, while a pressure transducer detects the air pressure and transmits the parameter signal to the NIBP input circuitry.

As the pressure is reduced, blood flows in the previously occluded artery, and changes the measurements made by the transducer. The point at which oscillation increases sharply is defined as systolic pressure. As the cuff continues to deflate, oscillation amplitude increases to a maximum, and then decreases. The peak oscillation amplitude is defined as the mean arterial pressure. The point at which the system detects a rapid decrease in oscillation is defined as the diastolic pressure.

10.6 SPO_2 PROCESSING

Measurement of oxygen saturation in the blood uses a specrophotometry technique. It is based on the facts that oxyhemoglobin and deoxyhemoglobin differ in the their absorption of red and infrared light, and that the volume of arterial blood in tissue changes during the pulse.

Using these facts, a pulse oximeter passes red and infrared light into an arteriolar bed and measures changes in light absorption during the pulsatile cycle. The light sources are red and infrared light emitting diodes (LEDs), while the detection is accomplished by a photodiode.

To identify the oxygen saturation of arterial hemoglobin, the monitor uses the pulsatile nature of arterial flow. During systole, a new pulse of arterial blood enters the vascular bed, and both blood volume and light absorption increase. During diastole, blood volume and light absorption reach their lowest point. The measurement is based upon the difference between maximum and minimum absorption, focusing on the pulsatile arterial blood.

In addition to the oximetry function, the input signals may be used to calculate heart rate.

10.7 TEMPERATURE PROCESSING

Measurement of patient temperature is accomplished by processing the signal from a probe containing a resistor whose impedance is temperature dependent. The class of such components is called thermistor.

The NPB-4000/C patient monitor is designed to accept the signals from electrically isolated Series 400 probes manufactured by Yellow Springs Incorporated. Interchangeable probes in this series may be used for esophageal, rectal, skin or surface, or airway temperature measurement. Probes are furnished with a standard 10-feet lead; extension leads are available.

The signal from the probe is conditioned by the monitor input circuitry, processed, and used to drive the numeric display.

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SECTION 11: ISOLATED FRONT END FUNCTIONS - THEORY OF OPERATION

11.1 Block Diagram
11.2 Overview
11.3 Interface Circuit
11.4 ECG
11.5 Respiratory Circuit
11.6 Temperature Circuit
11.7 Optocouplers
11.8 Controls
11.9 A/D Converter
11.10 Isolated Power Supply
11.11 SpO_2 Board
11.12 Isolation

11. ISOLATED FRONT END FUNCTIONS - THEORY OF OPERATION

11.1 BLOCK DIAGRAM

See Figure 11-1. The simplified block diagram of the previous section has been reproduced and highlighted to indicate the circuit block that will be described in some detail in the paragraphs that follow. As shown, the selected block is the isolated Front End circuitry. This block contains the interfaces with the patient connections at the input, and delivers an isolated output to the microprocessor and controller. An expanded block diagram for this circuitry is shown in Figure 11-2.

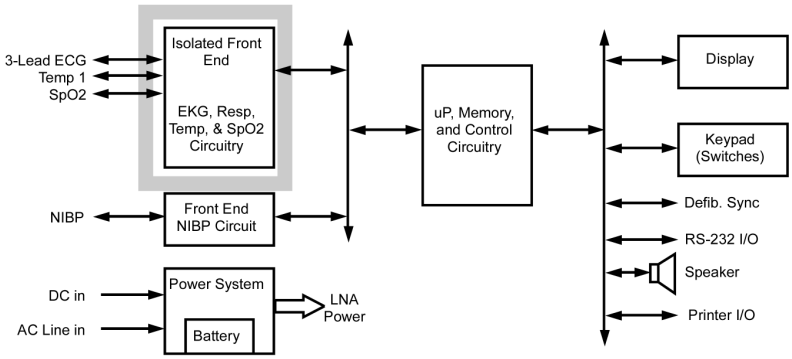

Figure 11-1: NPB-4000/C Simplified Block Diagram

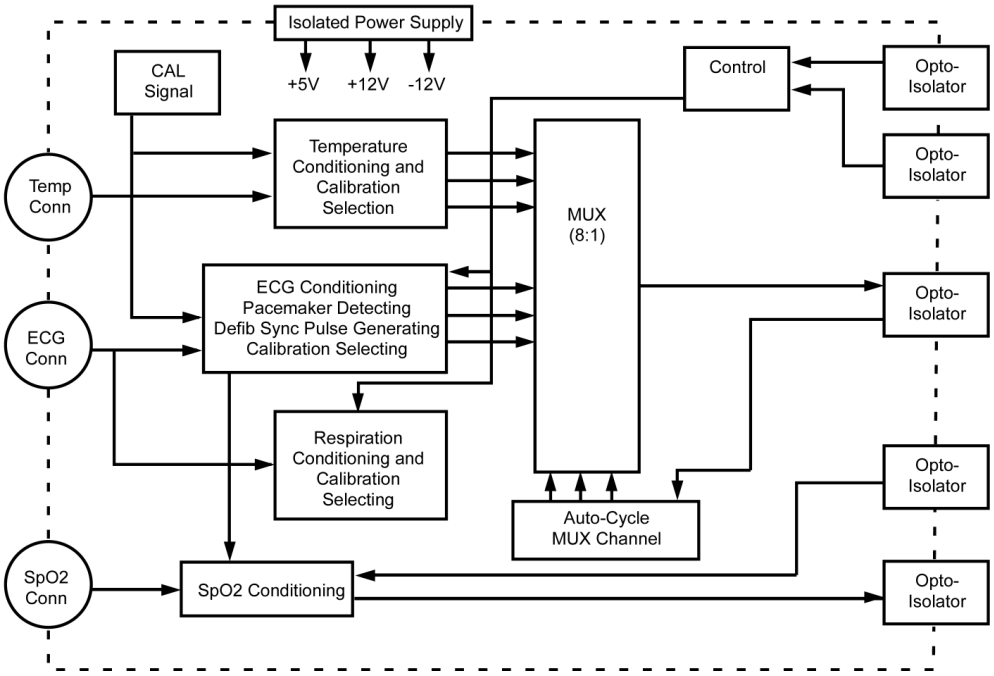

Figure 11-2: Isolated Front End Block Diagram

The NPB-4000/C Front End module is a part of the Main Board. It provides an isolation barrier between a patient's body and electrical potentials on the rest of the board as well as some high voltage protection of the isolation barrier itself.

11.2 OVERVIEW

The NPB-4000/C Front End Module consists of eight major blocks: interface circuit, ECG, respiration, temperature, controls, power supply, isolation, and A/D converter on the non-isolated side. It also carries an SpO_2 module which uses Front End for isolation and power supply.

- The ECG channel has 3-lead capability and a gain of 285. It provides two levels of low frequency noise filtering, T-wave filtering, R-wave detection, pacer detection capability and baseline reset.
- The temperature channel provides measurements over the range of 15 to 45˚C using YS400 series probes.
- The respiration channel incorporates the standard impedance pneumography method of injecting 100 kHz current of 42 micro Amps into a patient through the RA and LA leads and measuring voltage modulated by respiration on the same leads. Respiration can be measured in the range of 200 to 2000 ohms of a body impedance with the maximum modulation of 10 ohms.

- Isolation is provided by optocouplers. A total of four optocouplers are used for digital signals and a linear optocoupler with a multiplexer is used for all analog signals. The isolated side has its own power supply which generates +5 volts and -5 volts for analog circuitry and +5 volts for digital circuitry. A switching driver and an isolated transformer provide 100 kHz AC-power to the isolated side.
- An A/D converter on the non-isolated side digitizes signals coming from the linear optocoupler line as well as three signals from the NIBP circuit and other analog signals, such as samples of power supply voltages on the non-isolated part.

An expanded block diagram of the Front End is presented in the Figure 11-3.

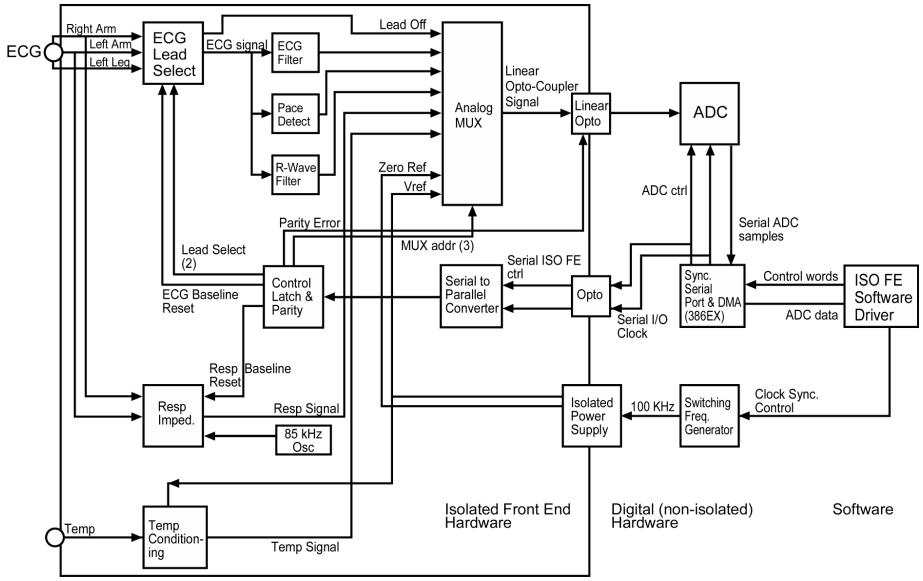

Figure 11-3: Front End Block Diagram, Expanded

Circuit descriptions that follow include reference designations of components identified in the Main PCB Schematic Drawing, Figure 17-7.

11.3 INTERFACE CIRCUIT

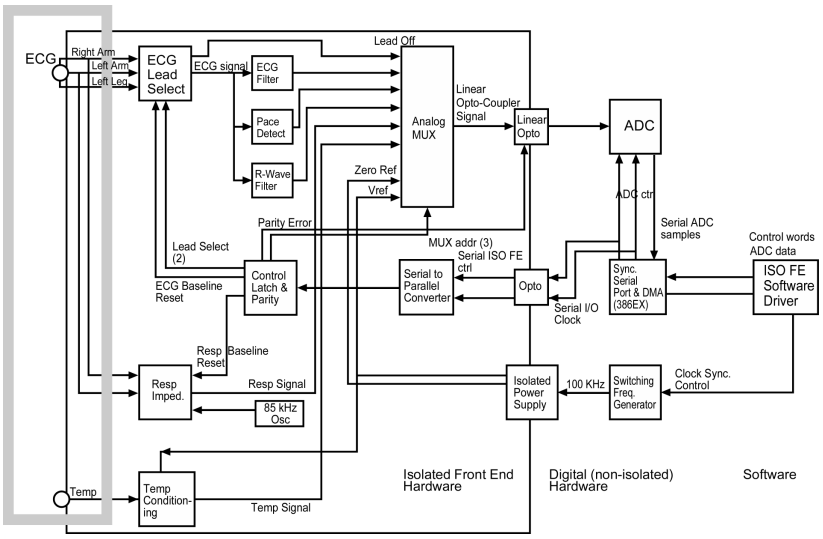

Figure 11-4: Interface Circuit Block Diagram

The interface circuit shown in the highlighted portion of the expanded block diagram, provides physical connection between patient connectors on the unit and preamplifier and other signal conditioning circuitry of the isolated Front End. It also incorporates ESD, defibrillator, and electrosurgery voltage suppression.

The instrument incorporates the standard ECG 3-lead system (I, II, III). The abbreviations RA, LA, and LL are the right arm, left arm, and left leg leads, respectively, and I, II, III are the potential differences between the limbs. The ECG signals through a patient cable are fed to a panel connector and through the panel harness to the board connector J11. All leads are protected by voltage suppressers. Suppressers D27, D25, and D24 are intended to clamp differentially applied defibrillation and voltages to around 160 volts, with the current limited to approximately 2.5Amps by two 1 kilo-ohm, 1W resistors installed in a standard ECG cable. The same suppressers will clamp ESD voltages close to 80 volts, relative to isolated ground. The R-C networks R278, C162, R279, C164, R254, C150; R261, C157, R247, C148, R246, and C146 provide further voltage and current limiting to the levels safe for inputs of the multiplexers having their own over-voltage protection of ±0.5 volts over supply voltages. The same R-C networks will provide for ESU and RFI attenuation and rejection of 100 kHz respiration signal in the ECG channel.

There are six other nets permanently connected to RA and LA leads. These are used for respiratory measurements. Two of them are connected to a high frequency source U81, two others to the inputs of signal followers U75C, and the last two, R121, C68 and R257, C178, are balancing LL to the isolated ground. The respiratory nets rely on the same suppression circuits as the main leads.

The temperature sensor signal is brought through a panel connector, and the common lead is connected to the reference through ESD voltage suppresser D23. Capacitors C131 and C136 are used to filter out RFI signals.

The SpO_2 sensor signal is brought through a panel connector and a separate panel cable to the board connectors J101 and J100. The Front End also has an SpO_2 output connector J10, into which the SpO_2 module (MP-205) is plugged.

11.4 ECG

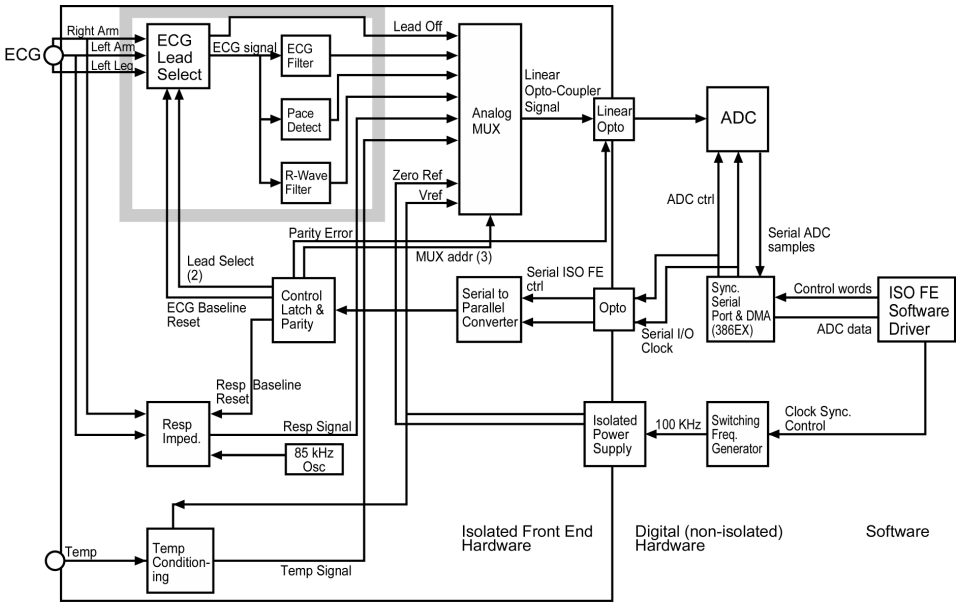

Figure 11-5: ECG Circuit Block Diagram

See Figure 11-5. As shown in the highlighted portion of the expanded block diagram, the ECG circuitry consists of the lead selection, preamplifier, amplifier and filter, R-wave detector, and pacemaker detector circuitry.

11.4.1 Preamplifier, Amplifier and Filter.

The ECG preamplifier connects to a patient via three leads. At any time, two of the leads are selected by the multiplexer U79 and connected to the inputs of the instrumentation amplifier U80 configured to have a gain of four. A common mode signal at the amplifier input is measured by the amplifier U75B, and used to drive the patient body via the amplifier U75A, resistor R291, and multiplexer U78 so that the common mode signal on the body and the output of the preamplifier would be eliminated. The amplifier U75B is also used for driving the shield with the common mode signal to eliminate capacitance loading.

The output of the drive amplifier U75A is used for leads-off detection. To implement this function, input leads of the differential amplifier are connected to the VDD supply through 20 megohm resistors R252 and R266. If any of the patient leads become disconnected from the body, the output of the drive amplifier U75A will go to a rail. A window comparator U77D is used to detect this event by producing a positive going signal sent to the A/D converter.

The preamplifier is followed by a 0.05 Hz high-pass filter made of capacitor C147 and resistors R248 and R249. The corner frequency can be changed by software to 0.5 Hz, set by resistors R238 and R250 and switch U63B. If a common mode charge on the capacitor C147 will offset the baseline to the point where ESG signal clipping is detected, it can be quickly removed under software control through the analog switch U63C and limiting resistor R239. The ECG circuit is completed by an amplifier U73B set for gain of 41 and a two-pole Chebychev low-pass active filter, U74C, with the cutoff frequency of 50 Hz and the gain of 1.75. The U74C has a +2.5 volts offset determined by resistors R225 and R236 to convert bipolar signals to unipolar format, as required by linear optocoupler. Thus, the total output swing of the ECG channel is about 1.5 volts.

11.4.2 R-wave Detector.

The ECG signal is further used to detect R-wave peaks. Active bandpass filter with U71A amplifier has the center frequency of 14 Hz and the passband of ±5 Hz. This filtering should eliminate false triggering in case of tall T-wave following R-wave. The signal is rectified by the full-wave rectifier made of amplifiers U71B and U71C, and dual-diode D13. This signal is used as one input to the comparator U74D. Sample-and-hold circuit consists of amplifier U71D, diode D17, capacitor C137, and discharge resistors R219 and R229. The resistors ratio sets the level of the comparator which goes to the positive rail when the next R-wave signal reaches the preset level of the previous R-wave signal held in the capacitor. The comparator signal turns on the monostable multivibrator U64A, which generates a 130-millisecond pulse. The pulse is sent to SpO_2 circuit and to analog multiplexer via divider R180, R186.

11.4.3 Pacemaker Detector.

Pacers are detected by the dV/dt circuit made of amplifier U74A, resistor R251, and capacitor C152. The circuit output will go to approximately ±1.4 volts when pacer is detected. This will set off the window comparator built around amplifier U74B and turn on monostable U64B to create an 8-millisecond pulse sent to the analog multiplexer via divider R179, R185.

11.5 RESPIRATORY CIRCUIT

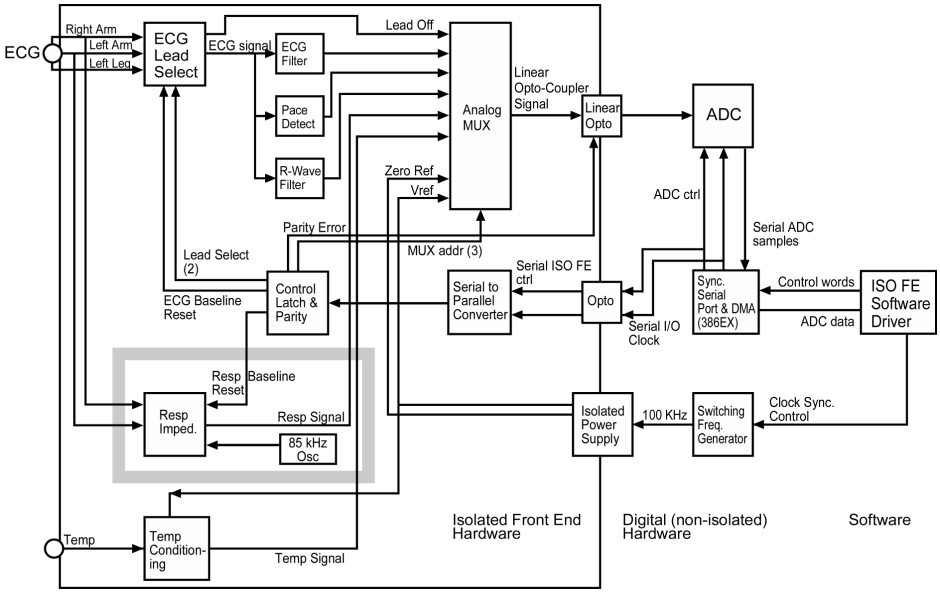

Figure 11-6: Respiratory Circuit Block Diagram

As shown in the highlighted portion of the expanded block diagram, Figure 11-6, the Respiratory circuitry includes the ECG leads, and some control circuitry.

Respiration is detected by measuring modulation of a high frequency AC signal sent to a body. The AC signal is 100 kHz, 4 volts peak square-wave complementary signals are produced by oscillator U81. These signals, via resistors R288 and R271, generate 42 microamps p-p current which is injected in a body through patient leads RA and LA. The AC voltage drop on these leads is respiration modulated and fed through high-pass filters C94, R244, C95, R228, and resistors R129 and R141 to a multiplexer U76 via buffers U75C and U75D. The multiplexer is controlled by the same AC signal that generates current and, in conjunction with amplifier U77C having gain of 9, comprise a synchronous detector.

The DC component of the filtered signal is removed by 0.1 Hz high-pass filter C134, C172, R205, and R204, and the remaining low frequency respiration signal is fed for further amplification. The capacitors C134 and C172 can be quickly discharged through U63D switch under software control in case of significant baseline drift. Amplifier U72B has a gain of 667 and creates +2.5 volts offset via resistors R215 and R216 to convert bipolar signals to unipolar format. Complete swing of the output is about 1.5 volts p-p, and the signal is fed to the linear optocoupler multiplexer.

11.6 TEMPERATURE CIRCUIT

The temperature is measured in the body range of 15 to 45˚C using Yellow Spring series 400 thermistor thermometers. Thermistor with the resistance range of 3539 to 984.2 ohms is connected as a feedback of amplifier U72A. The reference signal of 1.235 volts is supplied by voltage reference U70 through precision resistor R217. The temperature, therefore, is measured using output ratios. Other ratios have to be arrived at by using Yellow Spring thermistor value chart. Resistors R203, R218 and capacitor C130 comprise a low pass filter.

11.7 OPTOCOUPLERS

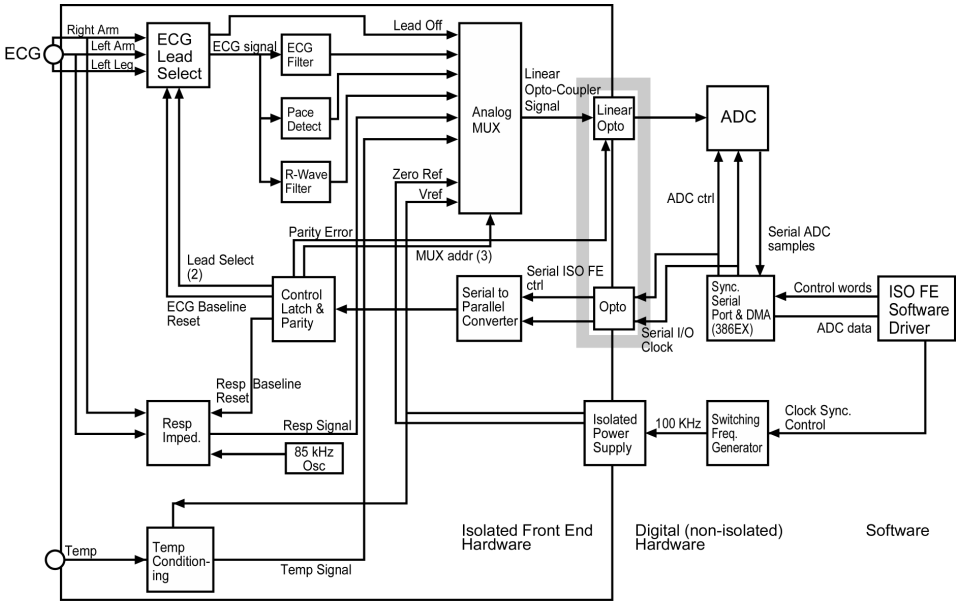

Figure 11-7: Optocouplers Block Diagram

See Figure 11-7. The optical couplers that isolate the Front End signals from the non-isolated digital hardware are of two types: Linear and Digital.

11.7.1 Linear optocoupler

All analog signals, ECG, Respiration, Temperature, VREF and AGND, as well as voltage levels of binary signals PM(pacemaker), QRS (R-wave), and LOFF(leads off) are fed to the inputs of analog multiplexer U67 and to the linear optocoupler U57. The optocoupler has an LED and two matched sensing photodiodes and works in a servo mode with two operational amplifiers, U60 and U51. Input current set by multiplexer output and resistor R166 is compared by U60 with the current of input photodiode. The LED is controlled by U60 until two currents are equal. The current of the output diode mirrors the input diode's current, thus producing an image of the multiplexer voltage at the output of U57. Operational amplifiers maintain very close to zero impedance at diode outputs, which provides for very linear diode currents and a very linear and stable current ratio. A small positive DC offset is provided from divider R168, R169 to compensate for possible amplifier negative voltage offset.

11.7.2 Digital Optocouplers.

Digital optocouplers are inverting, high-gain, low-power types. The baud rate is set for 50 kHz operation. Inverter U61 provides inversion of optocoupler signals.

11.8 CONTROLS

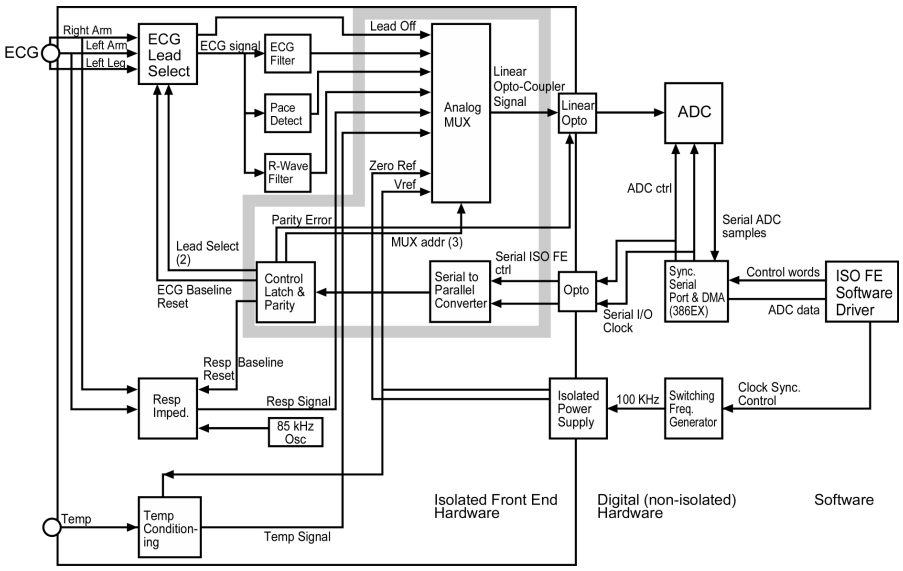

Figure 11-8: Controls Block Diagram

See Figure 11-8. The isolated control signals are developed and applied in the highlighted blocks as shown in the block diagram.

Front end operations are controlled by serial signals on ADCTX line clocked by signals on ADCCLK line. These serial signals from the Main Board CPU are fed to the Front End through opto-isolators U55 and U56 with pull-ups R182 and R173. Signals inverted by U61 go to eight-bit Serial-in/Parallel-out Shift Register U66. The beginning of a stream sets up one-shot retriggerable multivibrator U62A for the duration of 130 microseconds. The stream is 16 bits long, and each pulse retriggers the one shot. At the end of the stream, and after a 130 microseconds time-out, the parallel set of bits representing the last eight bits in the serial stream will be latched in an eight-bit buffer.

The bits represent different control functions. A group of three bits, MuxA, MuxB, and MuxC, control eight-bit data multiplexer U67; and a group of two bits, LSEL1 and LSEL2, control four-bit lead select multiplexers U79 and U78. Two others are individual bits, 0.5 Hz controls corner frequency of the high-pass filter, and ECGRES controls baseline reset.

The bit assignment is as follows(MSB first):

Bit 9 Parity
Bit 10 ECGRES
Bit 11 0.5Hz
Bit 12 LSEL2
Bit 13 LSEL1
Bit 14 MuxC
Bit 15 MuxB
Bit 16 MuxA

The parity bit is set for odd and is checked in the odd/even parity checker U65. Even parity, if detected, represents an error and the U65 output signal will turn on switch U63A. The switch will drive the output of U60 amplifier beyond the normal range of data signals and will set A/D output at all ones, which will be interpreted as an error.

Lead Select bits 12 and 13 select lead and test configurations as follows:

Bit 12	Bit 13	Selection
0	0	Test
0	1	Lead I
1	0	Lead II
1	1	Lead III

The mux address bits determine the following selections:

Bit 14	Bit 15	Bit 16	Selection
0	0	0	ECG
0	0	1	QRS
0	1	0	PM
0	1	1	RESP
1	0	0	LOFF
1	0	1	SCAL
1	1	1	AGN

11.9 A/D CONVERTER

A/D converter U53 on the non-isolated side is a 12-bit, 100 kHz sampling rate device with serial control and 14 analog inputs (3 are internal and 11 are external). It is configured for unipolar operation, 5 volts input and 16-bit cycle. The converter has four control lines: ADCS*(CS*), ADCRX(DATA/OUT), ADCTX(DATA/IN) and ADCCLK(I/CLK). Clock rate is set at 25 kHz. Each control burst is 16 bits long. The first eight-bit encode control information for the converter (MSB first) is: four-bit analog channel address (D7-D4), two-bit data length select (D3-D2), output format MSB or LSB first encode (D1) and unipolar or bipolar output select (D0). The last eight bits are ignored (they are used, though, to control operations of the isolated part).

When selected, the converter enables DATA INPUT and the I/O CLOCK and removes DATA OUT from the high impedance state. The I/O CLOCK shifts out data from the previous conversion and clocks in control bits for the current conversion. On the fourth falling edge of the I/O CLOCK the next channel selection is complete and the converter goes into the sampling mode. The falling edge of the 16^{th} I/O CLOCK puts data in hold, takes EOC low and begins the current conversion which lasts for 10 millisecond. If the selected channel is ISOAD the data comes from a channel of multiplexer U67, selected during previous serial burst. At least 80 microseconds delay is required between serial

bursts. This will provide enough time out for multiplexer control data to be latched. The multiplexer has at least four clock cycles of I/O CLOCK to settle before A/D sampling begins.

Data bits are assigned as follows:

	Input Data Bits				**Address Bits**			
	D7	**D6**	**D5**	**D4**	**LS1**	**LS2**	**LSBF**	**BIP**
Inputs:								
AIN0 — Isolated data	0	0	0	0				
AIN1 — NIBPPSR1	0	0	0	1				
AIN2 — NIBPPSR2	0	0	1	0				
AIN3 — OSC	0	0	1	1				
AIN4 —VBATTAD	0	1	0	0				
AIN5 — TEMAD	0	1	0	1				
AIN6 — +3.3VAD	0	1	1	0				
AIN7 — +12AD	0	1	1	1				
AIN8 — –24AD	1	0	0	0				
AIN9 — NC	1	0	0	1				
AIN10 — NC	1	0	1	0				
Internally connected inputs:								
(Vref+ — Vref–)/2	1	0	1	1				
Vref–	1	1	0	0				
Vref+	1	1	0	1				
Software power down	1	1	1	1				
Output data length:								
8 bits					0	1		
12 bits					X	0		
16 bits					1	1		
Output data format								
MSB first							0	
LSB first							1	
Unipolar (binary)								0
Bipolar (2s complement)								1

11.10 ISOLATED POWER SUPPLY

The isolated power supply consists of high-current switched driver, U54, isolation transformer T1, two full-wave rectifiers with dual diodes D11 and D10, filter capacitors C122 and C127 and three voltage regulators. Regulators U83 and U68 provide +5 volts and -5 volts for analog circuitry and regulator U69 provides +5 volts for digital circuitry on both Front End and SpO_2 boards. Switched driver U54 is controlled by square wave 100 kHz signals from the CPU and powered by the main power supply 12 volts regulator.

11.11 SPO_2 BOARD

The SpO_2 board (MP-205) plugs into the main board and uses it for power supply and isolation. The SpO_2 input signal through D-type panel connector and Front End connector J101 is fed to the receptacle J100; power, control, and output signals go to the receptacle J10. Two output signals are asynchronous: serial link RX and TX. Serial TX controls optocoupler U59, and RX is controlled by optocoupler U58. Control signal is ECG_SYNC which comes from the R-wave detector.

11.12 ISOLATION

The isolation barrier is provided by isolation transformer T1, linear optocoupler U57, and digital optocouplers U59, U58, U55, and U56. Spark gap SG1 is used to protect isolation components against over-voltage exceeding their limits.

SECTION 12: NIBP - THEORY OF OPERATION

12.1 NIBP System Overview
12.2 The Pneumatic Assembly
12.3 NIBP Hardware

12. NIBP - THEORY OF OPERATION

12.1 NIBP SYSTEM OVERVIEW

See Figure 12-1. The NPB-4000/C noninvasive blood pressure (NIBP) measurement and display operations described in this section include the pneumatics of the inflatable cuff and control valves, the specialized Front End NIBP circuitry, some of the microprocessor memory and control circuitry, some of the power system, and specific switches on the keypad. These are highlighted in the main system block diagram, as shown, with a distinction among the different shades of background tint to identify those that are only partly involved from the major circuitry dedicated to the NIBP functions.

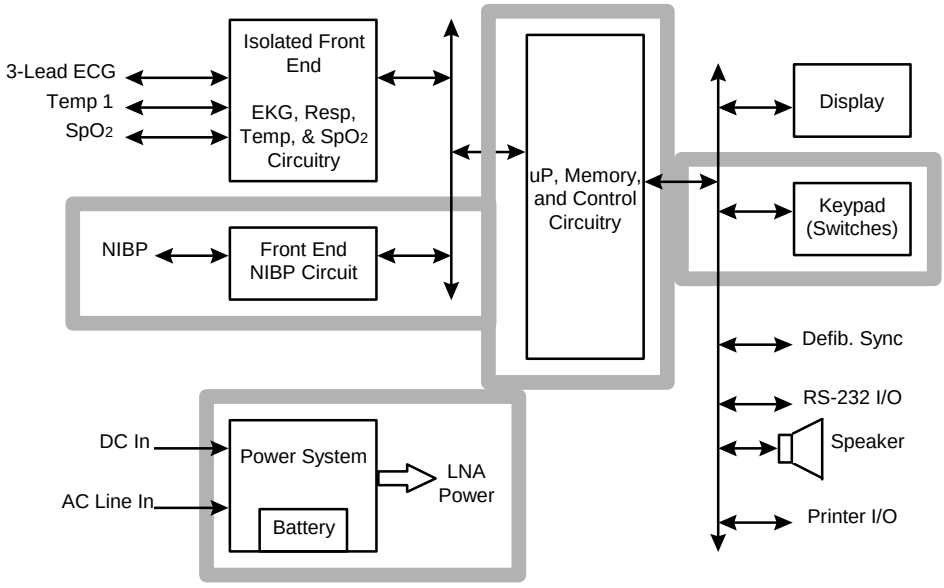

Figure 12-1: NPB-4000/C System Block Diagram

The major blocks involved from the cuff to the microprocessor are shown in the simplified block of the NIBP see Figure 12-2. The pump and motor, mounted on the power system assembly, are driven by a pulse-width-modulated (PWM) signal from the digital hardware section of the main board assembly. That signal is gated by an enabling signal originating in the microprocessor of the section of the main board. The pumped air is ducted through tubing and valves mounted on the main board and made available at the Front End connection to the cuff.

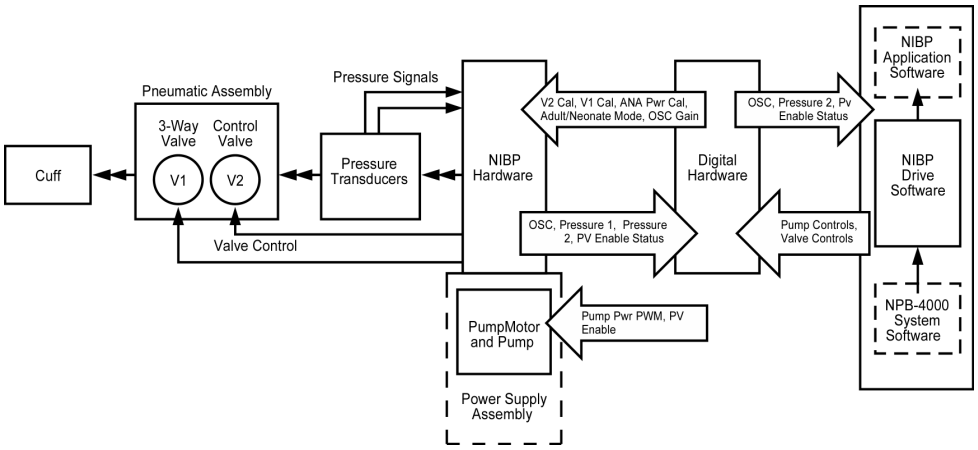

Figure 12-2: NIBP System Block Diagram

Prior to making blood pressure measurements, the cuff is placed around a limb, typically an upper arm (left or right). The NIBP measurement system is initiated by commands responding to pressing the NIBP Start/Stop switch on the front panel. The cuff is inflated at a rate controlled by the pump excitation current to a pressure above systolic, at which level the artery is effectively occluded. Then, as the cuff pressure is reduced at constant rate, the pressure transducers provide analog signals to the digital hardware where they are digitized and processed to obtain systolic, diastolic, and mean blood pressure values, as well as the beat rate.

The technique for translating the pressure signals into the required measurements makes use of the action of the oscillatory characteristic of the returning arterial pressure. The phenomenon is illustrated in the diagram below.

See Figure 12-3. Systolic pressure is defined as the point at which oscillation increases sharply. As the cuff deflates, oscillation amplitude increases to a maximum, and then decreases. The point of peak oscillation amplitude is the mean arterial pressure. The point at which oscillations cease is defined as the diastolic pressure

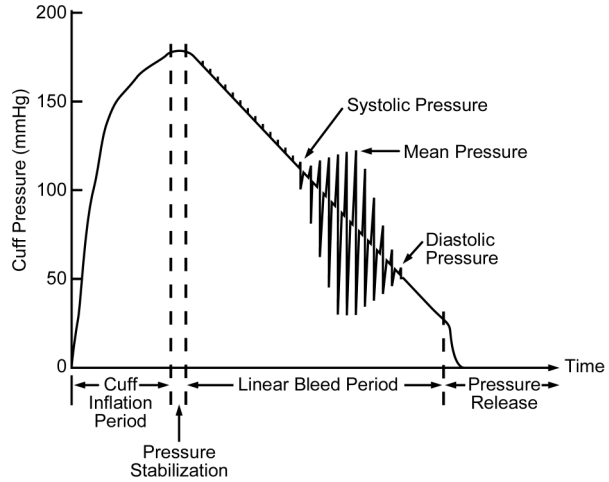

Figure 12-3: Oscillatory Characteristics Diagram

12.2 THE PNEUMATIC ASSEMBLY

The pneumatic assembly, consisting of the pump, two controlling valves, and tubing to connect the various pneumatic components together are illustrated in the schematic diagram that follows.

See Figure 12-4. The pump output is connected to the cuff and to two valves: a two-way proportional control valve (V2) and a three-way valve (V1), as well as to two pressure transducers. Operation of the valves and of the pump control are defined as described in the following text.

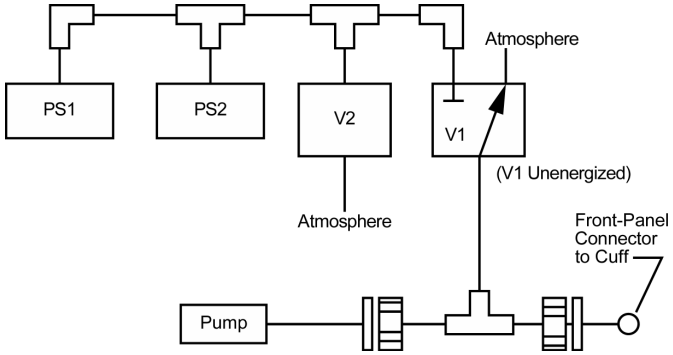

Figure 12-4: Pneumatic Assembly Block Diagram

Valve V1 is a three-way valve. In the V1 deenergized position, the portion of the pneumatic system encompassing the cuff and pump are open to the atmosphere, thus preventing the cuff from being pressurized. In the V1 energized position, the cuff and pump are connected to V2 and the pressure transducers. When V2 is closed, action of the pump will pressurize the cuff. Control valve V2 is used to bleed pressure from the cuff during an NIBP measurement, at a controlled deflation rate.

12.3 NIBP HARDWARE

See Figure 12-5. The NIBP analog control hardware is highlighted in the block diagram. It includes the Front End NIBP circuitry, as well as the pressure transducers and pump. Refer to the main PCB schematic drawing, Sheet 2, Figure 17-6, in connection with the circuit operation descriptions.

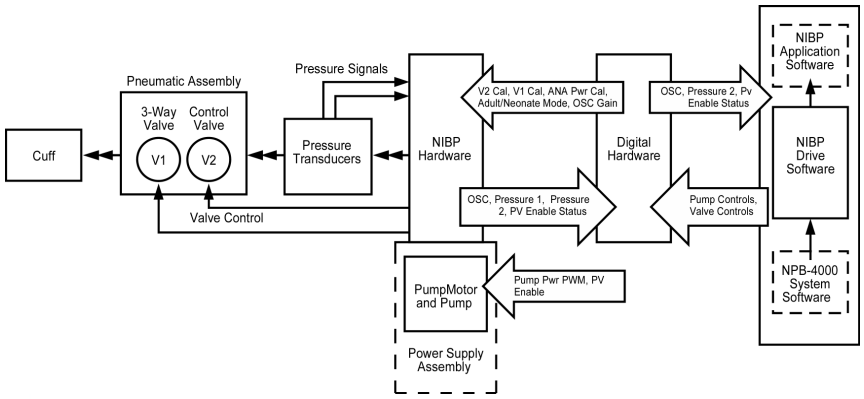

Figure 12-5: NIBP Hardware Block Diagram

12.3.1 Pressure Transducers

Pressure transducers PS1 and PS2 convert pneumatic pressure levels to voltages in the range from 0.33 volts at 0 mmHg to 4 volts at 300 mmHg. Transducer PS1 is used to sense the main cuff pressure. Transducer PS2 is used as a backup cuff pressure sensor, from which over-pressure warning signals are obtained. Both transducers outputs are smoothed to remove the effects of pumping pulsation. The output of PS1 is identified as signal NIBPPRSR1, while that of PS2 is NIBPPRSR2.

12.3.2 Filtering the Oscillatory Signal

Amplifiers U16-1 and U16-14, in combination with the lumped resistance and capacitance values of the passive components, form a band pass filter that separates and amplifies the oscillatory signals OSC from the deflating cuff transducer signal NIBPRSR1. Amplifier U16-8 provides hysteresis.

12.3.3 Power Supplies

Battery power, VBATTP, connected to the board at J3, pins 13 and 14, is regulated in U15 when that component is enabled by the NPANPWR analog power On/Off signal input to U10-4. The regulator accepts a battery voltage of 6 to 8 volts and delivers regulated +5 volts to power the pressure transducers and biasing circuitry for the operational amplifiers.

12.3.4 Over-Pressure Detector

Pump and valve drivers are controlled by the NPPVEN pump and valve enable signal that is generated in U16-7 level-detector amplifier circuit. One input to that amplifier is the NIBPRSR2 signal from transducer P2. The other is a value determined by voltage divider R68 and R64, and feedback resistor R61.

The pump and valve drivers are enabled only when cuff pressure is below nominal 330 mmHg for adult mode, and below 165 mmHg for neonatal measurements.

12.3.5 Pump and Valve Drivers

Three-way valve V1 coil is powered by VPS that is switched in series with the coil through n-channel MOSFET Q10-6. Switching action of Q10-6 is controlled by the input signal NP3WYV, that is gated by the enabling signal NPPVEN at switch U23. The VPS signal is developed from VBATTP through Q11-6 that is also controlled by NPVEN gating transistor Q6. Diode D5 acts to suppress voltage spikes. Resistor R101 ensures that Q10-6 will be OFF in case of an open to the input line. The valve is either fully closed, or fully open.

Control valve V2 coil is powered by VBATTP and controlled by switching n-channel MOSFET Q10-7 in series with the coil. Q10-7 is controlled by input signal NIBPCNTLVLV. Pulse width modulation (PWM) of a five-volt level is used to operate the control valve. No-voltage results in a fully closed valve. As the duty cycle of the PWM is varied from 0 to 100 percent, the valve changes smoothly from fully closed to fully open. Repetition rate for the PWM is at least 9 kHz. Diode D4 suppresses voltage spikes, and resistor R100 assures that Q10-7 will be OFF if the input line should open.

12.3.6 NIBP Pump Control

Note: The following description is duplicated in the Power Supply section. Reference designations for the two paragraphs that follow are found in power supply schematic drawing, Figure 17-3and Figure 17-4.

The power supply mechanical assembly holds the blood pressure pump and shield. The power supply contains circuitry that allows logic level control of the pump power from the processor board. For single-point fault protection, the pump requires two signals (PUMPON and PVENB to activate the pump. PUMPON (when high) turns on FET Q18 that pulls the bottom lead of the motor to ground. The PVENB signal through level translator Q19, turns on FET Q17 that pulls the top motor lead to VBATT.

When no voltage is present at Q18, the pump is fully off. As the duty cycle increases from 0 to 100 percent, the pump power changes smoothly from full OFF to fully ON. This control technique minimizes overshoot of the targeted pressure. Diode D32 suppresses voltage spikes, while R78 ensures that Q18 will be OFF if the line opens. Resistor R77 and capacitor C46 suppress motor brush noise.

12.3.7 Digital Signal Processing and Information Display

NPB-4000/C software, resident in the microprocessor controller and memory peripherals, include the algorithms needed to process the digitized outputs of the digital hardware just described. It also includes the system software that responds to the commands for desired modes of NIBP measurements, display of NIBP values of systolic, diastolic and mean arterial pressure, storing trend data, and for recording/printing of such data, and for initiation and silencing alarms. Details of these functions are contained in the theory of operation of the microprocessor and control circuitry.

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SECTION 13: MICROPROCESSOR COMPUTER AND CONTROL – THEORY OF OPERATION

13.1 General
13.2 Power Supply Connections
13.3 NIBP Processing
13.4 Recorder Operation
13.5 Isolated Front End Power Interface
13.6 SpO_2 Interface
13.7 Isolated Front End Power Signals
13.8 RS-232 Serial Port Interface
13.9 CPU Connections
13.10 Knob Interface Control
13.11 Push Switch Control
13.12 Digital Schematic Pages 1/2
13.13 Current Drain of Digital Electronics

13. MICROPROCESSOR COMPUTER AND CONTROL –THEORY OF OPERATION

13.1 GENERAL

The NPB-4000/C digital design is based on an Intel 386EX microcontroller, which has a 386SX microprocessor core and peripheral blocks around it. The internal peripherals are all controlled by on-board programmable registers. In order to save power, this design has a Vcc = 3.3 volts.

The data from the Front End (ECG, temp, resp) is multiplexed through a linear opto isolator to a 12-bit A/D converter, which is connected to the on-board synchronous serial port. The synchronous serial port is controlled by the on-board DMA unit.

The LCD display is a 640x480 black and white display that is connected to an S-MOS 1351FLB controller chip. This chip interfaces via the data bus to the 386EX. It has two 32kx8 SRAMs for data storage. The backlight is controlled by enabling +12 volts to the inverter board. The contrast for the LCD is controlled from the onboard -24 volts.

The main executable memory is a 256Kx16 flash memory which takes the upper 512k bytes of address space. This flash contains the boot program and the executable program for controlling the whole unit.

A 512-kbyte DRAM is located in lower memory starting at location 0 and is used for data storage and manipulation. The DRAM also has the ability to execute code when programming the flash with a new program from the external RS-232 port.

An RTC (real-time clock) chip is connected which keeps date and time of day. This unit has 64 bytes of battery-backed-up RAM; 14 bytes are used for the real-time clock (RTC), and 50 bytes are available for the software to use.

The recorder (thermal printer) and the external RS-232 port are controlled from software via a duart (dual serial port chip). These ports are the same as the com ports used on a PC and the duart is programmable via software.

The SpO_2 unit (MP-205) is connected to an asynchronous serial port via opto-isolators.

The push switches and rotating knob interface to the 386EX via the FPGA circuit. They are polled by the software at a 200-Hz rate.

The speaker is connected to an amplifier circuit, that is connected to a digital potentiometer. The programmable frequency is generated in the FPGA and connects to this programmable digital pot. The software controls the volume by programming this digital pot.

The defib sync pulse is bit-programmed via software and goes to the outside world via a digital driver.

The NIBP circuit is controlled by various port bits and control circuits in the ASIC.

13.2 POWER SUPPLY CONNECTIONS

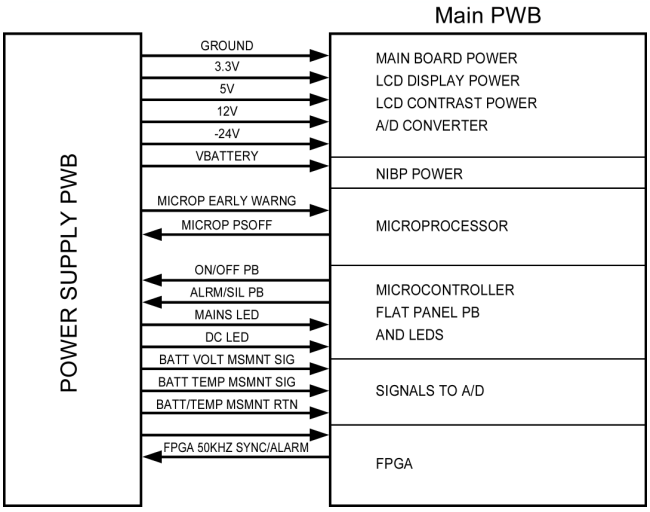

Figure 13-1: Power Supply Interface

See Figure 13-1. The power supply system provides the power for the main board and all of the circuitry in the system. It also contains control circuits for turning on and off the power, as well as supplying the battery backup for the system.

13.2.1 Voltages

The microprocessor and its associated circuits are powered from the regulated 3.3 volts generated on the power supply board. The 3.3 volts powers the microcontroller, DRAM, flash, LCD controller and a portion of the LCD contrast circuit, memory, the DUART, and real-time clock. The 5 volts powers the Nellcor knob, A/D converter, a portion of the LCD contrast circuit, and a portion of the speaker circuit. The 12 volts powers portions of the LCD contrast circuit and speaker circuit, the backlight inverter input voltage, and the op amp for the battery voltage and temperature-monitoring signals going to the A/D converter. The -24 volts is used to drive the LCD contrast regulator.

13.2.2 Microcontroller Signals

The battery and microcontroller have two signals that connect directly with each other, EARLY WARNING and PS OFF. The battery circuits generate an EARLY WARNING signal to the microcontroller that the power is going down within 100 millisecond. This EARLY WARNING signal could be due to the power On/Standby switch being depressed or from the battery voltage getting too low. The signal is connected directly to INTERRUPT 5 and INTERRUPT 7. The software will save any information it must save and finish its housekeeping before sending the PS OFF signal back to the battery circuits.

13.2.3 Membrane Switch and LED Signals

13.2.3.1 Membrane Switches Connected to the Power Supply

The power supply circuit connects directly with the ON/Standby switch and the two LEDs on the membrane switch. The On/Standby switch goes directly from the membrane switch to the power supply board. This is to allow powering up when off. Another switch, the Alarm Silence switch also goes to the battery circuit. Unlike the On/Standby switch, this switch also goes to the microcontroller.

13.2.3.2 Power Supply Generated LED Signals

The power supply circuits generate two LED driving signals, one that indicates that the AC mains is connected, and one that indicates that the DC power is connected. When the AC Mains LED is being driven on, a high voltage level goes to the 386EX port 1 bit 6 as the AC mains input status bit. When the LED is off, the signal is a logic low. The software will interpret the signal levels so as to tell whether the AC mains is connected or not. The same is true with the DC connector. The signal driving the DC LED goes to port 1, bit 7. This indicates the DC power status.

13.2.4 Battery Signals to the A/D Converter

The battery voltage and temperature signal is sent to the main board where it is buffered by an amplifier circuit that converts it to a signal within the 0-5 volts range of the A/D converter. The BATTSNS+ signal is sent directly to the Main Board and is divided by two by a resistor divider circuit on the positive input to the amplifier. The amplifier has a gain of two, which brings the signal back to its original signal level and then it is resistor-divided to the 0-5 volts range for the A/D converter.

13.2.5 Sync/Alarm 50kHz Signal

The power supply needs a 50 kHz signal to synchronize its own internal operation and to keep the alarm from sounding if the watch dog timer (WDT) times out. The 50 kHz signal is “anded” with the watchdog timer (WDT), and if the WDT should time out, the power supply circuit will sound the alarm and shut down the Main Board.

13.3 NIBP PROCESSING

See Figure 13-2. The NIBP circuits consist of microprocessor control for turning on and off certain signals, control logic generating the pump PWM and valve PWM, and status signals.

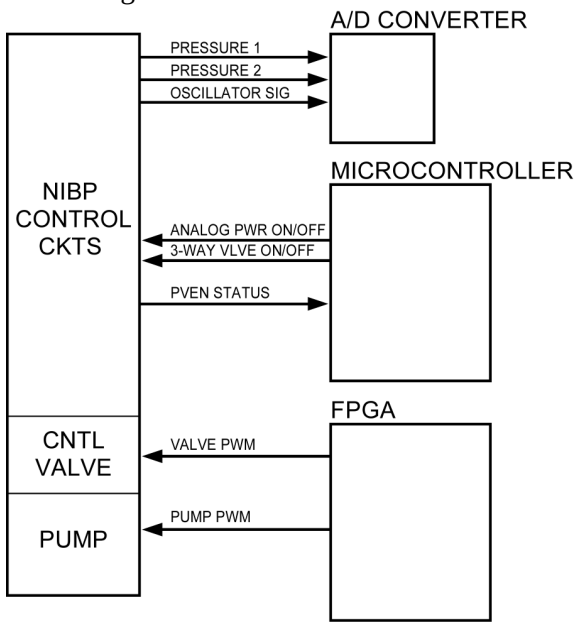

Figure 13-2: NIBP Processing Circuitry Block Diagram

13.3.1 NIBP Signals Going to the A/D Converter

The NIBP circuits generate three analog signals which must be converted to a digital code, the pressure from transducer 1, the pressure from transducer 2, and the oscillatory signal from pressure transducer 1. The signals are connected to the A/D converter for conversion and subsequent processing by the microprocessor.

13.3.2 Pressures 1 and 2

The pressure transducers output 0.33 volts at 0 mm-Hg to 4 volts at 300 mmHg. Transducer 1 is used for the main cuff pressure signal from which blood pressure results are calculated. Transducer 2 is used as the backup cuff pressure signals from which over-pressure warnings are obtained. These pressure voltages go to the A/D converter and are monitored by the software.

13.3.3 Oscillatory Signal

Transducer 1's signal is also filtered and amplified to separated cuff pressure oscillation signals that are present on the cuff pressure signal during the deflate portion of the measurement cycle. This signal also goes to the A/D converter and software algorithms detect the blood pressure systolic and diastolic values.

13.3.4 Microcontroller Control and Status Signals

There are five signals that interface directly with the microcontroller and NIBP circuits. Four of the signals are for control of the NIBP circuits from the microcontroller software and one signal is a status signal fed back to the software. All of the signals require 0-5 volts levels by the NIBP circuits, so each

of them is buffered by a logic gate that is connected to 5 volts. The inputs to these buffers are TTL-compatible and will switch when the input goes below 0.8 volts or above 2.4 volts.

13.3.5 Analog Power On/Off - Port 1 Bit 1

This signal turns on the power to the NIBP circuits via a regulator run from the battery. To turn on the NIBP circuits, port 1 bit 1 must be set by software to a high state.

13.3.6 3-Way Valve On/Off - Port 1 Bit 2

This bit controls the three-way pressure valve which is a back safety valve for the cuff pressure. A high signal allows a blood pressure measurement to occur, while a low signal dumps the air and the cuff is prevented from pressurizing.

13.3.7 Pvenable - Port 3 Bit 7

This bit is generated by the NIBP circuits for software monitoring of the over-pressure condition. Normal operation occurs when this signal is at a high level, indicating the cuff pressure is normal, while a low signal indicates an over-pressure condition.

13.3.8 Valve PWM Signal - FPGA

The FPGA control circuit produces a pulse-width modulated signal that is routed to the control valve for relieving the cuff pressure in an orderly manner for blood pressure measurement. The software programs an eight-bit register in the FPGA, which outputs a high pulse level for a programmable time, then a low level for a period of time. The high level is programmed by the software and the FPGA circuit automatically generates the low portion of the signal.

When this signal is low, the valve is fully closed. As the duty cycle of the PWM is varied from 0 to 100 percent, the valve changes smoothly from fully closed to fully open. The PWM repetition rate must be a minimum of 9 kHz. The circuit uses an eight-bit counter clocked at 5 MHz. This gives a 19.5 kHz programmable signal period, well above the 9 kHz minimum.

13.3.9 Pump Motor PWM Control Signal - FPGA

The software programs an eight-bit register in the FPGA circuit to generate a PWM control signal to the pump motor. When the signal is at a low level, the pump is off. A PWM signal is generated to turn on the pump in a smooth fashion by varying the duty cycle from 0 to 100 percent. There is an eight-bit counter that is clocked at 78 kHz. This gives a 304 Hz signal frequency for pump operation. Minimum pump PWM frequency for proper operation is 300 Hz.

13.4 RECORDER OPERATION

See Figure 13-3. The recorder is a thermal recorder option that is supplied by General Scanning Corp. This recorder has a self-contained microprocessor and control circuits for properly operating the recorder from commands sent to it via UART serial connection. The detailed operation of the recorder is specified in the operational manual supplied by the vendor.

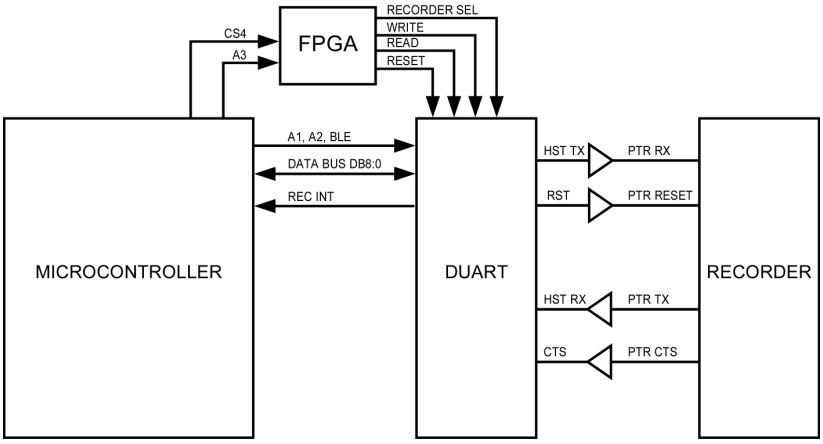

Figure 13-3: Recorder System Block Diagram

13.4.1 Recorder/Microcontroller Interface

The recorder is interfaced to the microcontroller via a DUART that has two UARTs programmed by the software. The DUART has a UART0 and a UART1, each with a full UART signal complement. The circuit uses UART1 of the DUART for the recorder interface. This UART has 16-byte fifos on each of the receive and transmit channels. The software programs the UART by setting the chip select unit, CS4 to I/O addresses for the recorder and then programming the internal registers for baud rate, parity, and bit count. Up to 16 bytes can be transferred to the UART, which will transmit serially to the recorder. The UART generates RS-232 signals in TTL/CMOS compatible signal levels. The recorder takes 0-5 volt signals, so each of the signals to/from the recorder must be translated from/to 3.3 volts/5 volts. This is done with the HCT244 buffers.

The UART signals and recorder signals are listed below.

Host transmit	-> printer receive
printer reset bit	-> printer reset
Host receive	<- printer transmit
Host CTS	<- printer clear to send

The host signals are generated by the programmable UART.

13.4.2 Recorder Power

The recorder requires 5 volts for logic operation and 10-18 volts for print head operation. The power for the recorder is generated on the power supply board and goes directly to the recorder from the power supply board. It is merged with the control signals to make one 50-pin cable going to the recorder interface board.

13.5 ISOLATED FRONT END INTERFACE

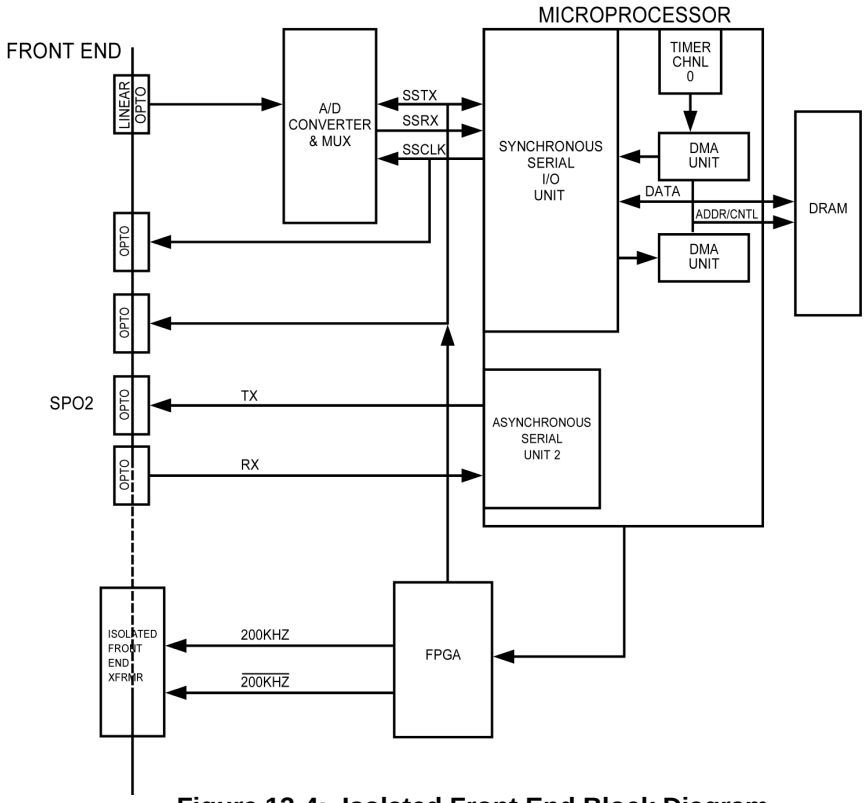

Figure 13-4: Isolated Front End Block Diagram

See Figure 13-4. The interface to the Front End electronics is shown above and consists of using the microprocessor's synchronous serial unit to interface to the A/D converter. The synchronous serial unit interfaces with the DMA unit, which passes the data to be transmitted to the A/D. The data received from the A/D goes to the other DMA channel and is transferred to a data buffer.

13.5.1 A/D Converter Transmit Control

The A/D converter initiates a conversion when it receives a serial stream from the microprocessor. The processor software sets up the DMA, synchronous serial unit, and timer channel 0 to work together to transfer control words to the A/D and Front End. The timer is set for a rate of 800 Hz and its output is programmed to go directly to the DMA unit. The DMA unit passes data from the DRAM to the SSIO unit, which in turn transmits the 16-bit word to the A/D and the Front End. The first eight bits transmitted are stored by the A/D and interpreted. A conversion starts. At the same time, the previous conversion is transmitted back to the SSIO unit (this is discussed in the next section). The last eight bits are read by the Front End and are used to select the Front End mux channel (three bits), initiate baseline reset (one bit), lead select (two bits), and select a 0.5 Hz filter (one bit). The eighth bit is a parity bit, which is checked by the Front End circuit. The software puts together a buffer with this data and programs the DMA channel to transmit the data words each time the timer generates a DMA request.

13.5.2 16-Bit Word Transmitted to the A/D Converter and Front End

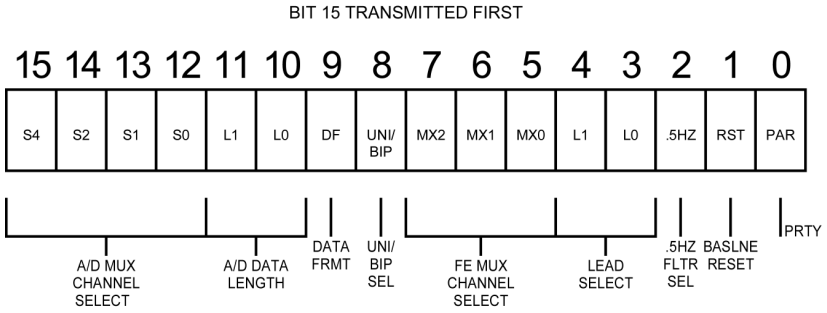

Figure: 13-5: 16 Bit Word

13.5.3 A/D Converter Receiver Control

The A/D converter is a pipelined converter and transmits the result of the previous conversion when receiving the next transmission for a conversion. The previous conversion is transmitted to the SSIO unit's receiver and the SSIO then requests a DMA transfer to memory.

13.5.4 SpO_2 INTERFACE

The microprocessor's asynchronous channel 2 (SIO2) is used to interface to the SpO_2 unit via opto-isolators. There are two signals, transmit and receive. This is a UART-type unit and when the SpO_2 transmits, the SIO receives the data and generates an interrupt to the software. When the software wants to transmit a byte to the SpO_2, it transfers data to the SIO transmitter and the SIO unit automatically transmits it to the SpO_2.

13.5.5 ISOLATED FRONT END POWER SIGNALS

The isolated Front End requires its own power supply and voltages, separate from the other voltages in the system. The FPGA generates a 100 kHz signal that connects to an isolation transformer. These signals are enabled/disabled by a bit in the CS5 control register. These signals are also connected to, and in synchronization with, the 50 kHz power supply clock. Resetting the Front End can be accomplished by turning the 100 kHz clock off, then back on again. This turns the Front End power supply off, then back on.

13.6 RS-232 SERIAL PORT INTERFACE

The RS-232 output serial port uses one of the asynchronous units of the DUART. It is programmed by the software using CS4 and the A3 address bit set to 0. This is done in the FPGA and output as DUARTCS0. The eight programmable registers are internal to the UART channel and are set up for baud rate, parity, number of bits to transmit, and start and stop bits. This channel also has an internal register with an extra bit. The circuit uses this bit as the NURSECALL signal on pin 9 of the RS-232 connector.

13.7 CPU CONNECTIONS

The processor in this system is a 386EX. The 386EX contains a 386SX core and integrated peripherals. It operates from a 40-MHz oscillator, and includes the following on-board peripherals:

DMA Controller Unit
Bus Interface Unit
Chip-select Unit
Clock and Power Management Unit
DRAM Refresh Control Unit
Watch Dog Timer Unit
2 Asynchronous Serial I/O Units
Synchronous Serial I/O Unit
Timer Unit with three 16-bit Counter/Timers
Interrupt Control Unit
Three 8-Bit Digital I/O Ports

The connections are as follows:

Address bus connects to the LCD controller, RTC address/data mux, DRAM address mux, and the boot and trend flashes. Six address lines go to the FPGA.

The data bus connects to the data bus buffers, which in turn connect to the DRAM, RTC, DUART, boot flash, trend flash, LCD controller, and the FPGA.

The address and data control signals are distributed to the FPGA, DRAM, RTC, LCD controller, boot and trend flashes, and DUART.

RESET comes from the FPGA.

CLK2 is a 40 MHz signal from the onboard oscillator.

13.7.1 Port 1 Signals

Port 1 is connected to the following signals:

1.1 NIBP analog power on/off - out
1.2 NIBP 3-way valve on/off - out
1.3 NIBP neonatal measurement - out - not used
1.4 LCD contrast up - out
1.5 LCD contrast down - out
1.6 AC mains input status bit - in
1.7 DC input status bit - in

13.7.2 Port 2 Bits

Port 2 bits used are as follows:

2.7 Speaker volume up/down select - out

13.7.3 Port 3 Bits

Port 3 bits used are as follows:

3.2 Defib key input - in
3.5 PSOFF - out
3.6 Defib sync pulse - out
3.7 NIBP PV enable - in

13.7.4 Chip Select Unit

The chip select unit has 8 chip selects and are defined as follows:

CS0: LCD control register select - eight-bit I/O
CS1: LCD memory select - 16-bit memory
CS2: Trend flash select - eight-bit memory
CS3: RTC select - eight-bit I/O
CS4: Duart select - eight-bit I/O
CS5: Misc. control/status registers - NIBP control, switch status, and speaker tone control - eight-bit I/O
CS6: DRAM select - 8/16-bit memory
UCS: Executable flash select - 16-bit memory

There are wait states associated with each of the CSU's selects, and they are defined as follows:

CS0: read/write - six wait states
CS1: read/write - six wait states
CS2: read/write - four wait states
CS3: read/wrote - 18 wait states
CS4: read/write - two wait states
CS5: read/write - no wait states
CS6: read/write - one wait state
UCS: read - two wait states/write - four wait states

13.7.5 Timer Unit

The timer unit has three timers: two are used for output control, and one is used to initiate DMA transfers to the A/D converter.

TIMEROUT0: Speaker volume adjust pulse
TIMEROUT1: A request for initiating an A/D conversion
TIMEROUT2: 100 kHz output to the FPGA for generating the 100 kHz and 50 kHz signals for the power supply

13.7.6 Interrupts

There are five interrupts used:

INT1: DUART channel 1 interrupt
INT2: DUART channel 2 interrupt
INT5: Early warning from the power supply (Also connected to INT 7)

13.7.7 Synchronous Serial Port

The synchronous serial port is connected to the A/D converter. The signals used are as follows:

STXCLK:	synchronous transmit clock
SRXCLK:	synchronous receive clock
SSIOTX:	synchronous transmit data
SSIORX:	synchronous receive data

The STXCLK signal is generated in the FPGA circuit each time Timer 1 initiates a pulse (1.25 millisecond intervals). There are 16 clock pulses generated by enabling a 25 kHz signal to the STXCLK line. The A/D is programmed for 16-bit transfers, and when the A/D receives the 16th clock, it will activate the EOC signal that turns off the STXCLK signal. The A/D makes a conversion and passes the data back the next time it receives the STXCLK signal. The SRXCLK signal is connected to the STXCLK, and each time a new conversion is initiated, the previous conversion's data is transferred to the 386EX via the SSIORX data line.

13.7.8 Asynchronous Serial Port

There are two asynchronous UART ports on the 386EX, but only one is used. It is connected to the opto-isolators that connect to the SpO_2 unit.

TXD0: asynchronous transmit signal
RXD0: asynchronous receive signal

The remaining port is reserved for future use.

13.7.9 Watch Dog Timer Unit (WDT)

See Figure 13-6. The watchdog timer unit within the 386EX has one output which goes to the FPGA.

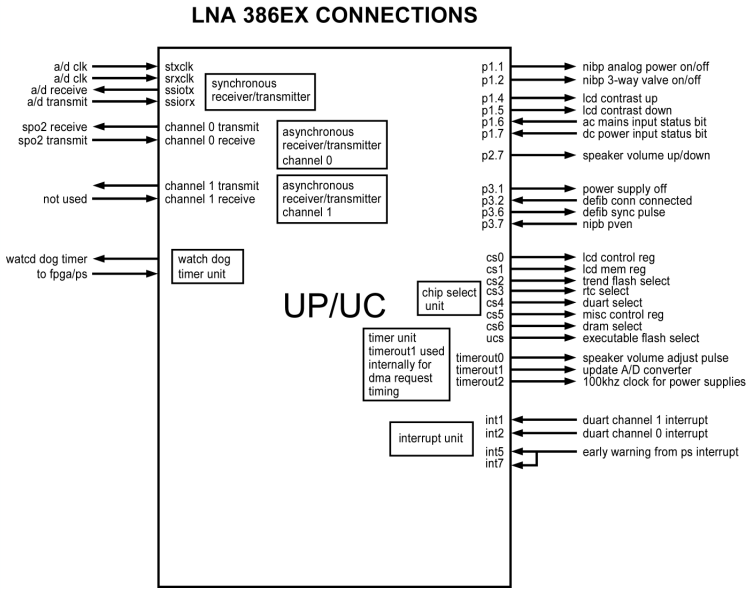

Figure 13-6: Watch Dog Timer Block Diagram

13.7.10 CPU Timing Signals

The 386EX runs from a 40 MHz crystal oscillator and the main timing is derived from this clock. It is called CLK2. Inside the CPU, CLK2 is divided by two, generating two new clocks, PH1 and PH2. Each T state is made up of one PH1 and one PH2 clock. There are a minimum of two T states per cycle. Each wait state is one T state long (50 nanosecond) Therefore, adding wait states is adding 50 nanoseconds for each additional T2 states.

13.7.11 CPU Signals

Various signals change at various times within a cycle, and the generic timing is shown below. Some of the key signals are ADS#, M/IO#, D/C#, W/R#, WR#, RD#, CS0-CS6#, BLE#, and BHE#. Typical control circuits will look at ADS# at the end of PH2 and make decisions at this time. See Figure 13-7.

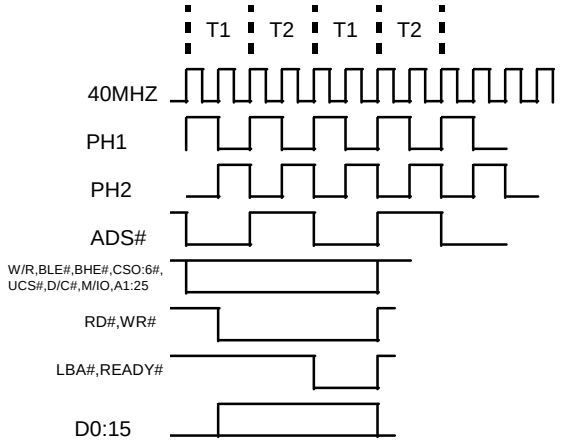

Figure 13-7: CPU Signals

13.8 DRAM Control

The DRAM control consists of one 256kx16 DRAM chip, three 74ACT157 address mux chips, address resistors, and the FPGA control circuit.

The CS6***** (* = # = a low true signal) signal has been assigned to the DRAM memory address space: 0-3FFFF words, or 0-7FFFF bytes. The CS6***** control register in the chip select unit (CSU) must be programmed for one wait state. Since the data bus is 16 bits wide and the DRAM is a x16 part, most transfers will be of the 16-bit variety. However, eight-bit transfers are allowed and provisions have been made for byte addressing. This is done by using the upper and lower cas signals, UCAS and LCAS.

13.8.1 DRAM Signals

For the DRAM design we must generate six signals, RAS#, UCAS#, LCAS#, DRAMOE#, DRAMWR#, and CASADREN. All of these signals are generated in the FPGA from the 386EX signals, ADS#, CS6#, M/IO#, D/C#, WR#, and RD#. Since the CSU is programmed for one wait state, the CSU generates the READY# signal, which terminates the transfer.

13.8.2 DRAM Timing

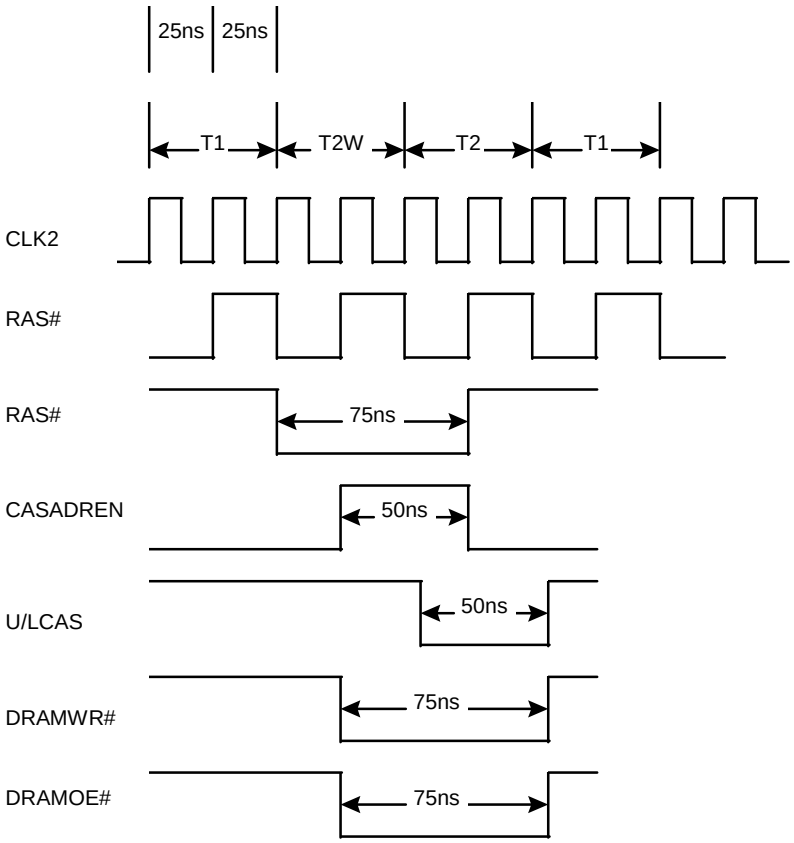

Figure 13-8: DRAM Timing

See Figure 13-8. The DRAM requires 130 nanoseconds total time, read/write and precharge for each cycle. There is one wait state for each DRAM access and a total of three T states, which is 150 nanoseconds. Since the DRAM minimum access time is 130 nanoseconds, we have 20 nanoseconds of margin. The Hitachi HM51W4260AL has a RAS* time of 70 nanoseconds, a precharge time of 50 nanoseconds, a CAS* time of 20 nanoseconds, and a WE* time of 15 nanoseconds. The BLE* and BLH* signals are used to select byte-oriented reads and writes. There are two CAS* lines that are used to implement the byte writes.

The RAS# and CAS# requirements are shown in Figure 13-9.

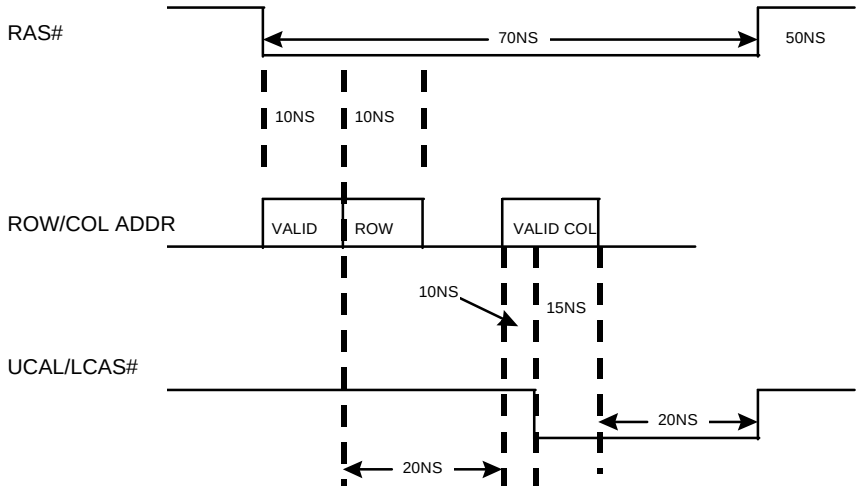

Figure 13-9: RAS# and CAS# Requirements

13.8.3 DRAM FPGA Circuits

The DRAM control circuits in the FPGA must decode the various 386EX control signals and generate the DRAM signals. This is done by using CS6# to set a flip flop when ADS# and PH are true. The flip flop is RAS#. This signal is passed to two more flip flops and the RAS# output is 75 nanoseconds long. This signal is generated for all DRAM accesses and refresh. The DRAM output is enabled when either BLE# or BHE# is true, which means a read is occurring. Since the DRAM outputs are bi-directional, we need to disable the DRAMOE# signal if a write is taking place. The WR# signal being false allows DRAMOE# to occur. If it is true, then the DRAMWR# signal occurs. The BLE# and BHE# signals are also used to generate the UCAS# and LCAS# signals during a read or write operation. Since we are using RAS only for refresh, the CAS signals must be inhibited for refresh.

13.9 Flash Control

The flash memory and control consists of two flash chips, a bootable flash (also called the executable flash) and a trend flash. The control consists of the random logic in the FPGA. The bootable flash is a 256Kx16 Intel (part no. E28F400BVT60) or Micron (part no. MT28F400 SG-8) flash with the boot in the top section (T), and is preprogrammed on the data I/O or some other unit with the boot program. The executable program can also be programmed this way or by downloading it to the 386EX via the RS-232 connection. The trend flash consists of Atmel AT29LV256 32kx8 devices that store the trend data and that write 64 bytes at a time. It takes two wait states for reading the flash, either the executable or the trend, and four wait states to write either of these flashes.

13.9.1 Executable flash

The executable flash is a word-oriented flash, that is, reading and writing is done on a word basis, and byte reads and writes are not allowed. The trend flash is byte oriented and all reads and writes are done on a byte basis.

The chip select unit has UCS* assigned to the executable flash and CS2* is assigned to the trend flash. Typically, the executable flash is assigned the upper 256k words, or 512k bytes in the system. The word address space is 40000 to

7FFFF, which is 80000 to FFFFF in bytes. This is the upper portion of the space. The trend flash is assigned to the 32k byte space above the video ram, that is, 84000 to 8FFFF words, or 11000 to 14000 bytes. The software, however, has the ability to overlap the trend flash address with the executable flash address. The design gives priority to the trend flash address over the executable flash.

The executable flash has a long delay time for writing to it, and this is why there are four wait states. It also has a long delay from output data on to output data float. This requires that data buffers be installed between the 386EX and the flash. Since doing this only for the flash is awkward, the buffers were put in for all external devices.

See Figure 13-10. The read cycle time for the executable flash is 110 nanoseconds. The write pulse width must be at least 150 nanoseconds. Refer to the timing diagrams for the flash for minimum timing parameters.

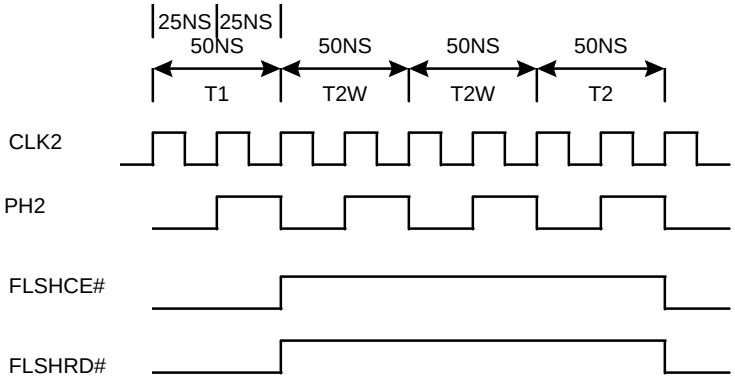

Figure 13-10: Flash Cycle

In the FPGA control logic, the executable flash chip select, is anded with the trend flash chip select such that **CS2*** must be high, inactive, when addressing the executable flash. This allows the address overlap for the trend flash. The executable flash chip enable, FLSH1CE#, is generated in the FPGA and then goes to the executable flash. The trend flash is connected directly to CS2#, because it has priority over the executable if an overlapping addressing scheme is used.

See Figure 13-11. The write pulse width is generated via a state machine to give the proper pulse width.

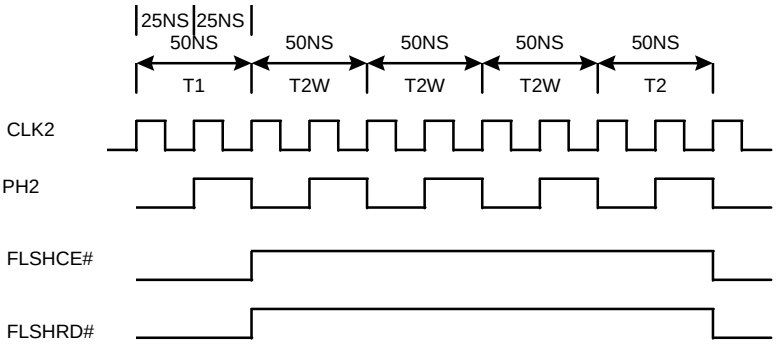

Figure 13-11: Write Pulse

13.9.2 Flash FPGA Control Circuit

The FPGA decodes the boot flash and trend flash select signals and generates the boot flash (FLSH1CE#) signal whenever the trend flash is not being accessed. Since the trend flash address space may overlap the boot flash space, the trend flash has priority.

The flash outputs are enabled for a read cycle. During a write cycle, the data bus inputs data to the flash.

Since the boot flash is for booting up and executing the software program, most accesses to the boot flash are reads. Only when a new program is downloaded will a write to the boot flash occur.

13.9.3 Trend Flash

The purpose of the trend flash is to store the patient's data. It has both read and write accesses occurring at regular intervals. The flash chosen for this purpose interfaces with the 386EX easily, and writing data consists of transferring 64 bytes at a time. The flash takes care of any erasing and writing operations internally. Typical worst-case write/erase times for 64 bytes is less than 1 second.

13.10 LCD Display

The LCD display is a black and white (B&W) 640x480 pixel display, used as a 1-bit/pixel B&W display. Gray shading is not used in this display. It is a dual panel, dual drive unit and the 1351 drives the display directly. It operates from 3.3 volts.

The LCD display is divided into two sections: each section is 640x240 pixels, which equals a total of 153,600 pixels per section. A 32Kx8 SRAM has 256,000 bits, thus one SRAM is used for each of the display sections. Only one bit is available to drive each pixel. For shading or color, more memory is needed.

The SRAM access time is defined by the 1351FLB as one over the frequency minus 20 nanoseconds.

tacc = 1/fosc - 20 nanoseconds

Our system uses an oscillator frequency (FOSC) = 10 MHz, therefore, 80 nanoseconds access time on the SRAM is needed. Using this SRAM and 10 MHz, the worst-case access time is 4 TOSC + TCLK = 500 nanoseconds.

The LCD display interfaces to the S-MOS LCD controller chip, SF1351FLB. This controller chip is connected to the 386EX and two 32kx8 SRAMs. The LCD controller has control registers that must be set up by software before writing to the memory and display.

13.10.1 LCD Control

There are two chip selects assigned to the LCD display chip: one for the control registers inside the chip, and one for the display memory space. The chip itself has a state machine controller inside, and generates the necessary signals to store and retrieve data from the memory when requested. It also takes care of driving the LCD display directly, with the data from the display SRAM.

The circuit uses the 1351 in mode 5 and the 16-bit microprocessor interface configuration. All transfers are word oriented, and byte reads and writes are not allowed.

The processor interface consists of the following signals.

IOCS# is the control register chip select and connects directly with CS0# from the 386EX. To program the 1351 registers, the software selects this address and transfers the data.

MEMCS# is the display memory select signal. It is connected to CS1# directly and display data is transferred to the display ram using this address space.

IORD#, IOWR#, MEMRD#, and MEMWR# are used to read and write to/from the control registers and the display memory. The two read signals are connected directly with the RD# signal from the 386EX. The two write signals are connected directly with the WR# signal from the 386EX.

The MPUCLK is connected to a 10 MHz clock generated in phase with the PH1 clock in the FPGA. Since PH1 occurs at the beginning of each 386EX T state, the 1351 will be in synch with the 386EX.

RESET is connected directly with the RESET signal from the FPGA, which goes to the 386EX.

The MPUSEL signal is tied to 3.3 volts via a resistor. This indicates that the 1351 is to operate in word mode.

The BHE# signal is connected directly to the BHE# signal from the 386EX.

AB0-AB15 is connected to the address bus of the 386EX.

DB0-DB15 is connected to the bi-directional data bus BD0-BD15.

The above signals are all of the signals used to interface to the 386EX for transferring of data to and from the control registers and the display RAM.

Both read and write transfers between the 386EX and the 1351FLB are defined in the 1351FLB manual, pages 1-33 and 1-34. The timing specifications of the 1351FLB for reading and writing data to and from the control registers or display RAM, allow a direct interface to the 386EX. External control circuits in the FPGA are not necessary, except for one signal, the READY# signal. This is explained in a following section.

13.10.2 LCD Display RAM

The interface signals for the display RAM are prefaced with the letter V, which indicates video RAM. The interface to the display RAM (VRAM) is defined in the 1351FLB manual and is connected directly to the RAM.

The LCD display interfaces directly with the 1351FLB. Timing diagrams are in the associated manuals. The signals used are LCDENB, XSCL, LP, WF, YD, UD0-UD3, and LD0-LD3. The UD and LD signals are data lines to the upper and lower display panels. The XSCL is the data shift clock and the LCD display stores the data on the falling edge of this clock. The LP signal is the latch pulse and is used to latch the data into the X-drivers. The YD signal is the frame pulse, which indicates a start-of-frame.

13.10.3 LCD FPGA Control Circuits

The LCD display chip interfaces directly with the 386EX. The only circuit that is necessary to generate in the FPGA is the READY# circuit. The 1351 generates a wait signal when transfers are initiated. This wait signal is gated with the LCD select signals and implements an external READY signal when the 1351 has completed the transfer.

13.11 Real-time Clock (RTC)

The RTC is a Dallas DS1693, which has the crystal and battery imbedded in the unit. It is a 28-pin DIP package and runs from a 3.3 volts supply.

CS3# is assigned to the RTC in the I/O space and the software must assign 14 wait states to this unit.

The timing for the DS1693 is shown in Figure 13-12.

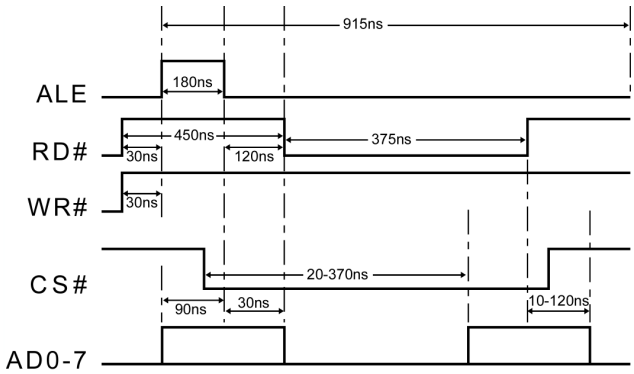

Figure 13-12: DS1693 Timing

See Figure 13-13. The timing for this interface is done in the FPGA. There is a state machine that is clocked at 20 MHz and generates 18 states.

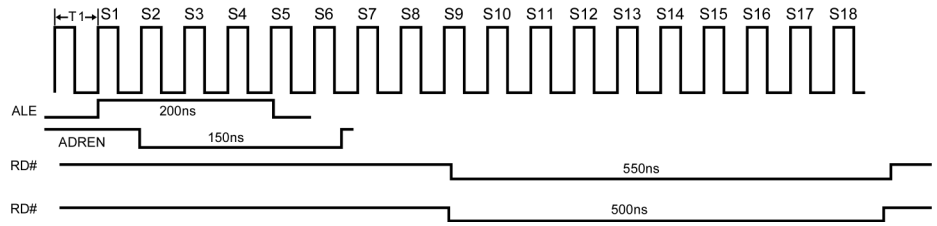

Figure 13-13: Interface Timing

13.12 DUART Control

See Figure 13-14. The DUART is a Startech ST16C2550CJ44 which consists of 2 UARTs and fifos for the read and write portions of each UART. Channel 0 is assigned to the RS-232 port, which exits the unit near the AC and DC inputs. Channel 1 is assigned to the recorder. The fifos are 16 bytes deep, and transfer to/from the DUART would save time if done on 8- or 16-byte boundaries.

Interfacing to the DUART is done by assigning CS4# to the DUART I/O space, with four addresses assigned to each UART. The DUART channel 0 is the base address assigned to CS4# and the channel 1 address is the base address + 8 (A3). There are four addresses assigned to each UART, 0,1,2,and 3.

Software must program two wait states for CS4# and define them as a byte device.

A state machine in the FPGA is used to generate the proper signals for programming the unit.

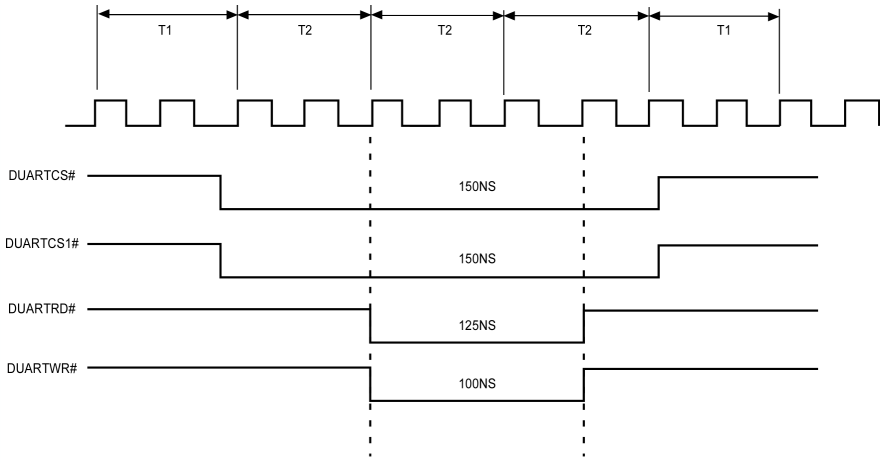

Figure 13-14: DUART Control

13.13 KNOB INTERFACE CONTROL

The knob consists of a rotary knob with a push switch. The knob is rotated and the cursor on the LCD display moves forward or backward, depending on which way the knob is rotated. When the knob is pushed, it must be detected and indicated to the 386EX.

The knob has two channels: channel A and channel B. When clockwise rotation occurs, channel A leads channel B and when counterclockwise rotation occurs, channel B leads channel A. The software monitors the knob flip flop, and when it is set true, the knob has turned. The direction is read by the other bits in the status register, and the software determines the knob direction. The KNOBINT flip flop is reset by the software when a write to CS5# + A occurs. The knob direction is determined by the software by reading CS5# + A, bits 4 and 5.

The circuit that drives the knob is a 3.3 volts circuit, with appropriate resistor values to allow the same current at 3.3 volts through the optocouplers as would have occurred at 5 volts.

13.14 SWITCH CONTROL

There are five switches and one knob push-button switch. All of these switches go to the FPGA control circuit except for the On/Standby switch, which goes directly to the power supply control circuit. Each of the switch circuits has a debounce resistor and capacitor associated with it and then goes to the FPGA. The signals ALRMSIL, NIBPPB, AUDTONVOL, LCDCONTRST, and KNOBPB go to the FPGA where they are OR'd together and exit as PBINT. This is read by the software in the status register. The software debounces and detects the length of time the switch is depressed. The software determines which switch was depressed by reading CS5# + A, bits 4 through 7.

13.15 MISCELLANEOUS CONTROL - CS5#

The NIBP PUMP PWM, NIBP VALVE PWM, SPEAKER FREQUENCY DUTY CYCLE, and a miscellaneous control register are all assigned to the I/O space programmed to CS5#. The addressing scheme is as follows:

CS5#	NIBP PUMP PWM	8 bits
CS5# + 2	Not used	
CS5# + 4	SPEAKER HIGH VALUE	8 bits
CS5# + 6	SPEAKER LOW VALUE	8 bits
CS5# + 8	CONTROL REG	8 bits
CS5# + A	WRITE RESETS KNOB INT/READ PUSH SWITCHS and the KNOB ROTATION DIRECTION bits	
CS5# + C	WRITE WDTEN (WATCHDOG TIMER ENABLE)/READ PUSH SWITCH SWITCHES AND THE KNOB PUSH BUTTON	
CS5# + E	WRITE NSCALL (BIT 7) and/or PTRRST (BIT 6)/RAD NSCALL and PTRRST	

13.15.1 CS5# NIBP Pump PWM 8 Bits

The NIBP pump pulse width modulated (PUMP_PWM) signal is generated in the FPGA via an eight-bit register which is clocked at 313 kHz. An eight-bit value is loaded into this register, and then the PUMP_PWM_GO bit (bit 0) in the CONTROL REG. is set true, and the pump PWM signal begins. The eight-bit register starts counting down, and the signal output is low until the counter underflows, at which time it is reloaded with the programmed value. It now counts up, and the signal output goes high until the counter overflows. It is then reloaded and counts down. The PUMP_PWM signal is generated this way until it is shut off by resetting the PUMP_PWM_GO bit in the control reg.

The NIBP valve pulse width modulated (NIBPCNTLVLV) signal is generated in the FPGA via this same eight-bit register, which is clocked at 313 kHz. An eight-bit value is loaded into this register, and then the VALVE_PWM_GO bit (bit 1) in the control reg. is set true, and the valve PWM signal begins. The eight-bit register starts counting down, and the signal output is low until the counter underflows, at which time it is reloaded with the programmed value. It now counts up, and the signal output goes high until the counter overflows. It is then reloaded and counts down. The NIBPCNTLVLV signal is generated this way until it is shut off by resetting the VALVE_PWM_GO bit in the control reg.

13.15.2 CS5# + 4 Speaker High, CS5# + 6 Speaker Low Value

The speaker tone frequency is generated using two eight-bit registers, one which is the value for the high portion of the frequency and one value for the low portion for the frequency. The frequency range is 200 Hz to 1000 Hz. The 16-bit counter has a selectable count frequency of 78 kHz or 313 kHz. This selection is programmed in the control reg. using the CLK_FREQ_SEL (bit 2). Signal A 0 selects 313 kHz and a 1 selects 78 kHz. Once the values are loaded, and the frequency clock is selected, the FREQ_GO bit (bit three) is set to begin the tone frequency. Software has complete control over the duty cycle of this tone by programming the high and low values and being able to select the clock frequency for the counter. The TONE_OUT signal is low until the low counter overflows and sets the TONE_OUT flip flop high. Now the high counter is enabled, and the TONE_OUT signal stays high until the high counter overflows, at which time it goes low and the low counter begins counting. This cycle continues until the FREQ_GO bit is reset to zero.

13.15.3 CS5# + 8 Control Register

This register has eight programmable bits as follows:

BIT 0 PUMP_PWM_GO
BIT 1 VALVE_PWM_GO
BIT 2 CLK_FREQ_SEL
BIT 3 FREQ_GO
BIT 4 BCK_LITE_ON
BIT 5 FRONT END CLOCK ENABLE
BIT 6 PORGQM FLASH ENABLE
BIT 7 ADCS RESET

Bits 0 through 3 were defined in the above paragraphs and need no further explanation here. Bit 4, BCK_LITE_ON is a bit that turns on the LCD backlight when set to a 1. When powered on, this bit is 0 and the backlight is off. To turn on the backlight this bit must be set to a 1.

Bit 5 enables the clock going to the Front End transformer, that generates the isolated Front End voltages. If the Front End should ever go into a baseline condition, it is reset by stopping the clock to the transformer, and the Front End voltage will go to zero. Turning this bit back on powers the Front End up and, essentially, acts as a reset.

Bit 6 enables programming of the boot flash. This would be used if a new executable program were downloaded via the RS-232 channel and stored in the executable flash.

Bit 7 resets the A/D converter and is generated when software starts a conversion sequence.

13.15.4 CS5# + A RESET KNOB INT/READ PUSH SWITCHS

The I/O address of CS5# + 6 has two functions associated with it. Writing to this register generates a KNOB_INT_RST signal which resets the knob interrupt flip flops. This would be done by software after a knob interrupt occurs.

The software polls this register every 50 millisecond and looks to see if the PB INT bit (bit 6) or the KNOB INT bit (bit 7) is set true, indicating that a switch has been pressed or that the knob is being rotated. If either of these bits is set true, then the software just looks at bits 3, 4, and 5 to determine which of the knob functions has occurred. If the PB INTB is set true, then register C must be read to determine which switch has been pushed.

Register CS5# + A has the following bit assignments:

Bit 0 Not used
Bit 1 Not used
Bit 2 Not used
Bit 3 Knob push button switch
Bit 4 Knob channel B rotation
Bit 5 Knob channel A rotation
Bit 6 Push Button occurred
Bit 7 Knob rotation occurred

13.15.5 CS5# + C Write Enables WDT/READ Push Buttons

After powering up, the software must enable the watch dog timer function by writing to this register. The act of writing to CS5# + C automatically sets the WDT flip flop to a 1 and enables the WDT time out function.

Reading this register gives the push-button status, as well as the state of the WDT flip flop.

Register CS5# + C has the following bit assignments:

Bit 0 Not used
Bit 1 Not used
Bit 2 Not used
Bit 3 WDTEN (Watch Dog Timer Enable)
Bit 4 LCD Contrast switch
Bit 5 Audio Volume switch

13.15.6 CS5# + E WRITE NSCALL/PTRRST/READ PUSH SWITCHS

Writing to this register sets or resets the nurse call and printer reset bits. To set NSCALL**,** write a 1 to bit 7, and to reset NSCALL write a 0 to bit 7. To reset the printer, write a 1 to bit 6. To reset this bit write, a 0 to bit 6.

The bit assignments for reading this register are shown below. The bit assignments for writing the NSCALL and PTRRST are different from the read assignments.

Register CS5# + E has the following bit assignments

Bit 0 Not used

BIT 1 Not used

BIT 2 Not used

BIT 3 Not used

BIT 4 Not used

BIT 5 NURSE CALL

BIT 6 PRINTER RESET

BIT 7 PRINTER **CTS** (CLEAR TO SEND)

The NURSECALL and PRINTER RESET bits are the flip flop outputs programmed by writing to register CS5# + E as explained above.

A 1 (high) indicates that the bit is true, a 0 that the bit is false.

13.16 DIGITAL SCHEMATIC FIGURE 17-5 THROUGH FIGURE 17-7

These schematics include all of the above circuits and some additional circuits that need explanation. For clarity purposes we will discuss the page 1 and integrate page 2 wherever necessary.

Page 1 of the schematics is mostly the digital portion of the design. It contains the following chips:

386EXMP	microcontroller
ACT1000F	programmable device with the control circuits
LCD CONTROLLER	1351FLB LCD display control chip
74HCT244	buffer chips for the signals from the LCD controller to the display itself
74LVC16245	data bus buffer to interface the 386EX to the other chips
RTC DS1693	real-time clock with 64 bytes of battery-backed ram and on-board crystal
74LVC541	mux for the address/data to the RTC
DUART	dual UART for the RS-232 and recorder
MAX211E	RS-232 interface chip with 15,000 volts ESD
DISPLAY RAM	32K x 8 SRAM for the LCD display
DRAM	256K x 16 dynamic ram memory
74ACT157	address mux for the DRAM
BOOT FLASH	bootable/executable flash memory
TREND FLASH	flash memory for storing trend data
OSCILLATOR	40 MHz oscillator to generate CLK2

Page 2 of the schematics contains the NIBP circuits, the speaker circuits, the LCD contrast circuit, the battery voltage and temperature input circuits, the push-switch interface circuit, and the backlight interface connector circuit. The 50-pin connector connects to the recorder, RS-232 connector, the power supply connector, the defib connector, and the speaker.

The speaker circuit consists of a software-programmable digital potentiometer chip, U28, which is a Dallas DS1666S-10. The software sets the tone frequency by setting the high register with a value, setting the low register with a value, then programming the digital potentiometer up/down according to the timing specified in the requirement specification.

13.16.1 Block Diagram

See Figure 13-15. The following diagram is a block diagram of the digital section of the NPB-4000/C design.

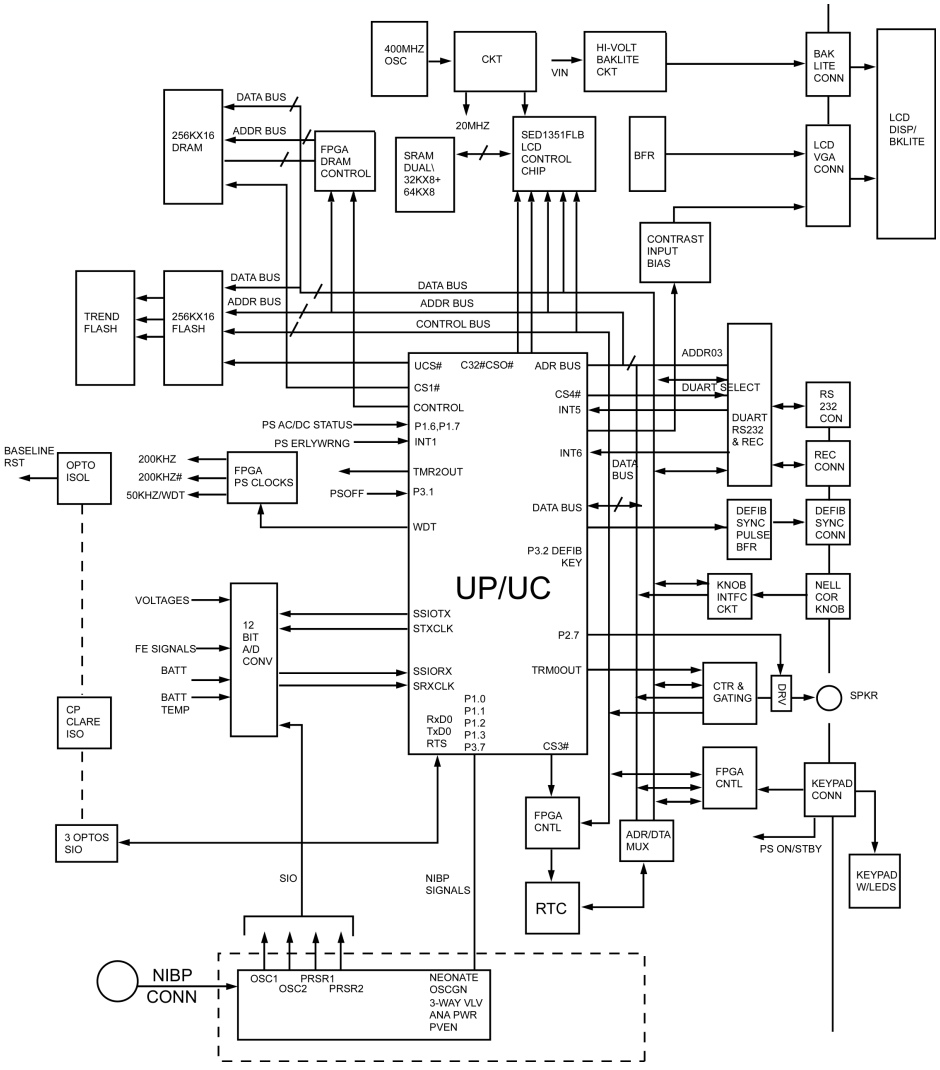

Figure 13-15: Digital Section Block Diagram

13.17 CURRENT DRAIN OF DIGITAL ELECTRONICS

The current drain has been determined by using the maximum numbers in the data sheets of the devices. Typically, the devices operate significantly lower.

386EX	130 mA
4M DRAM	95 mA
4M FLASH	30 mA
LCD CNTLR	20 mA
256k SRAM	50 mA x2 = 100 mA
DUART	3 mA
RS232 XCVR	5 mA
256k FLASH	15 mA
RTC	15 mA
40MHz osc	9 mA
Subtotal =	**422 mA**
misc. logic	78 mA
Grand Total =	**500 mA**
Available Power = 3.3 volts x 500 mA = 1.65 W	

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SECTION 14: MAIN COLOR BOARD DIGITAL THEORY OF OPERATION

14.1 General
14.2 Power Supply Connections
14.3 CPU Connections
14.4 LNA 386EX Connections
14.5 CPU Timing
14.6 Dram Control
14.7 Flash Control
14.8 LCD Display
14.9 Real Time Clock (RTC)
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14.13 Miscellaneous Control - CS5#
14.14 Speaker
14.15 NIBP (Non Invasive Blood Pressure) Control
14.16 Front End Interface
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14.18 Block Diagram
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14. MAIN COLOR BOARD DIGITAL THEORY OF OPERATION

14.1 GENERAL

The LNA color digital design is based around an Intel 386EX microcontroller, which has a 386SX microprocessor core and peripheral blocks around it. The internal peripherals are all controlled by on board programmable registers. In order to save power this design has a Vcc = 3.3 volts.

The data from the front end (ECG, temperature, respiration, etc.) is multiplexed through a linear opto isolator to a 12 bit A/D converter, which is connected to the on board synchronous serial port. The synchronous serial port is controlled by the on board DMA unit.

The LCD display is a 640x480 TFT color display which is connected to an S-MOS 1354F0A controller chip. This chip interfaces via the data bus to the 386EX and has one 1MX16 DRAM for data storage. The backlight is controlled by enabling the +12 volts DC to the inverter board. There is no contrast adjustment for this display.

The main executable memory is a 512Kx16 flash memory which takes the upper 1Megabyte of address space. This flash contains the boot program and the executable program for controlling the whole unit.

A 2 Megabyte DRAM is located in lower memory starting at location 0 and is used for data storage and manipulation. The DRAM also has the ability to execute code when programming the flash with a new program from the external RS-232 port.

A RTC (real time clock) chip keeps the date and time of day. This unit has 64 bytes of battery backed up ram, 14 bytes are used for the RTC, and 50 bytes are available for the software to use.

The recorder (thermal printer) and the external RS-232 port are controlled from software via a DUART (dual serial port chip). These ports are the same as the COM ports used on a PC and the DUART is programmable via software.

The SpO_2 unit (MP205) is connected to one of the 386EX's asynchronous serial ports via opto-isolators.

The push buttons and rotating knob interface to the 386EX via the FPGA circuit. They are polled by the software at a 200 Hz rate.

The speaker is connected to an amplifier circuit which is connected to a digital potentiometer. The programmable frequency is generated in the FPGA and connects to this programmable digital potentiometer. The software controls the volume by programming this digital pot.

The DEFIB SYNC pulse is bit programmed via software and goes to the outside world via a digital driver. The DEFIB SYNC pulse's purpose is to indicate on the leading edge that now is the time to fire the defibrillator.

The NIBP circuit is controlled by various port bits and control circuits in the ASIC. It automatically inflates a pressure cuff attached to the patient and then deflates the cuff and takes the measurement.

The main board uses the following voltages and nominal currents; 3.3 volts DC at 300 mA, 5 volts DC at 260 mA, 12 volts DC at 315 mA with 165 mA for the backlight, and -24 volts DC at 1.2 mA.

The IC's and their reference designations are as follows:

386EX, U7
40MHZ OSC, X3
A/D CONV, U53
AUDIO POT, U26
BOOT FLASH, U504
CONTRAST POT, U18
DATA BUS BUFFER, U9
DRAM, U501
DRAM ADR MUX, U2,U6,U8
DUART, U24
FPGA, U505
LCD CONTROLLER, U500
LCD VRAM, U502
MISC BFRS, U1,U12,U17
OP AMPS, U27,U16,U25
PRSR XDCRS, PS1,PS2
RS232 BFR, U19
RTC, U4
RTC ADR MUX, U3
TREND FLASH, U14
VOLTAGE REG, VR1

14.2 POWER SUPPLY CONNECTIONS

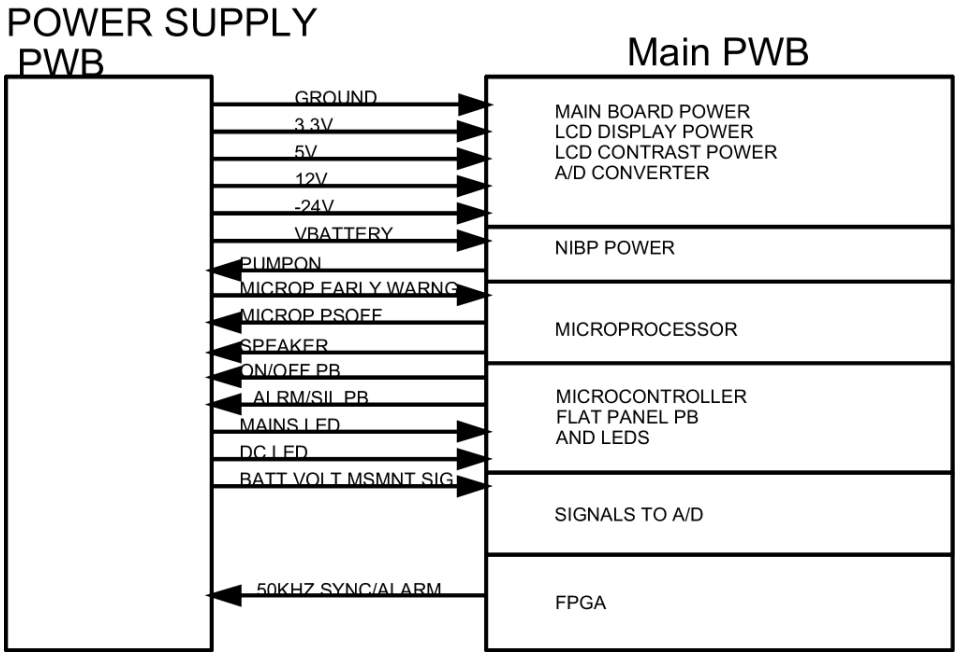

Figure 14-1: Power Supply Connections

The power supply provides the power for the main board and all of the circuitry in the system. It also contains control circuits for turning on and off the power, as well as supplying the battery backup for the system.

14.2.1 Voltages

The microprocessor and its associated circuits are powered from the regulated 3.3 volts DC generated on the power supply board. The 3.3 volts DC powers the microcontroller, DRAM, flash, LCD controller and a portion of the LCD contrast circuit, memory, the DUART, and real time clock. The 5 volts DC powers the Nellcor knob, the TFT color display, and a portion of the speaker circuit. The A/D converter is powered by its own 5 volt regulator. The 12 volts DC powers the speaker circuit, the backlite inverter input voltage, and the op amp for the battery voltage going to the A/D converter. The -24 volts is not used. Typical current draws are as follows:

3.3 volts DC @ 300 mA
5.0 volts DC @ 260 mA
12.0 volts DC @ 315 mA
-24 volts DC @ 1.2 mA

14.2.2 Microcontroller Signals

The power supply circuit and microcontroller have 2 signals which connect directly with each other, EARLY WARNING and PSOFF. The battery circuits generate an EARLY WARNING signal to the microcontroller to warn it that the power is going down within 100 ms. This EARLY WARNING signal is generated if the power *On/Standby* switch is pressed or the battery voltage gets too low. The signal is connected directly to INTERRUPTS 5 and 7. The software will save any information it must save and finish its housekeeping before sending the PSOFF signal back to the battery circuits.

14.2.3 MEMBRANE SWITCHES/POWER SUPPLY

The power supply circuit connects directly with the *On/Standby* switch and the 2 LED's on the membrane switch. The *On/Standby* switch goes directly from the membrane switch to the power supply board via the 50 pin cable. This is to allow powering up when off. Another switch also goes to the battery circuit, the A*larm Silence* switch. Unlike the *On/Standby* switch, this switch also goes to the microcontroller.

14.2.4 POWER SUPPLY GENERATED LED SIGNALS

The power supply circuits generate two LED driving signals, one that indicates that the AC mains is connected, and one which indicates that the DC power is connected. When the *AC MAINS* LED is being driven on, a high voltage level goes to the 386EX port 1 bit 6 as the AC mains input status bit. When the LED is off the signal is a logic low. The software will interpret the signal levels so as to tell whether the AC mains is connected or not. The same is true with the DC power input connector. The signal driving the DC led goes to port 1, bit 7. This indicates the DC power status.

14.2.5 BATTERY SIGNALS TO THE A/D CONVERTER

The battery voltage signal is sent to the main board where it is buffered by an amplifier circuit which converts it to a signal in the 0-5 volt range of the A/D converter. The BATTSNS+ signal is sent directly to the main board and is divided by 2 by a resistor divider circuit on the positive input to the amplifier. The amplifier has a gain of 2, which brings the signal back to its original signal level and then we resistor divide it to the 0-5 volt range for the A/D converter.

14.2.6 SYNC/ALARM 50KHZ SIGNAL

The power supply needs a 100 kHz signal to synchronize its own internal operation and to keep the alarm from sounding. The 100 kHz signal is "anded" with the watch dog timer (WDT) and if the WDT should time out the power supply circuit will sound the alarm and shut down the main board.

14.3 CPU CONNECTIONS

The CPU (U7) is a 386EX microcontroller, which contains a 386SX core and various integrated peripherals. The 386EX operates from a 40 MHz oscillator (X3) and has the following on board peripherals:

- DMA Controller Unit
- Bus Interface Unit
- Chip-select Unit
- Clock and Power Management Unit
- Dram Refresh Control Unit
- Watch Dog Timer Unit
- Asynchronous Serial I/O Units
- Synchronous Serial I/O Unit
- Timer Unit with 3 16 Bit Counter/Timers
- Interrupt Control Unit
- Bit Digital I/O Ports

The 386EX's address bus connects to the LCD controller **(**U500**)**, RTC address/data mux (U3), DRAM address mux (U2, U6, U8), and the boot **(**U504**)** and trend flash **(**U14**)**. Six address lines go to the FPGA **(**U505). The 386EX's data bus connects to the data bus buffers, which in turn connect to the DRAM (U501), RTC (U4), DUART (U24), boot flash, trend flash, LCD controller, and the FPGA. The 386EX's control signals are distributed to the FPGA, DRAM, RTC, LCD controller, boot and trend flash, and DUART. Reset to the 386EX is generated in the FPGA**.**

CLK_40MHZ is a 40 MHz signal from the on board oscillator.

14.3.1 PORT 1 SIGNALS

Port 1 is connected to the following signals:

1.0	NU
1.1	NIBP analog power on/off - out
1.2	NIBP 3-way valve on/off - out
1.3	NIBP neonatal measurement - out
1.4	NU
1.5	NU
1.6	AC mains input status bit - in
1.7	DC input status bit - in

14.3.2 PORT 2 BITS

Port 2 uses one bit.

Speaker volume up/down select - out

14.3.3 PORT 3 BITS

Port 3 bits used are as follows:

3.2	Defib key input - in
3.5	PSOFF - out
3.6	Defib sync pulse - out
3.7	NIBP PV enable - in

14.3.4 CHIP SELECT UNIT

The chip select unit has 8 chip selects and are defined as follows:

CS0:	LCD control register select - 8 bit I/O
CS1:	LCD memory select - 16 bit memory
CS2:	Trend flash select - 8 bit memory
CS3:	RTC select - 8 bit I/O
CS4:	DUART select - 8 bit I/O
CS5:	Misc. control/status regs - NIBP control, push button status, and speaker tone control 8 bit I/O
CS6:	DRAM select - 8/16 bit memory
UCS	Executable flash select - 16 bit memory

There are programmable wait states associated with each of the CSU's selects and they are defined as follows:

CS0:	read/write - 2 wait states
CS1:	read/write - 2 wait states
CS2:	read/write - 4 wait states
CS3:	read/write - 18 wait states
CS4:	read/write - 2 wait states
CS5:	read/write - no wait states
CS6:	read/write - 1 wait state
UCS:	read - 1 wait state/write - 4 wait states

14.3.5 TIMER UNIT

The timer unit has 3 timers, 2 are used for output control and 1 is used to initiate DMA transfers to the A/D converter.

TIMEROUT0:	Speaker volume adjust pulse
TIMEROUT1:	DMA request for initiating an A/D conversion
TIMEROUT2:	100 kHz output to the FPGA for generating the 100khz and 50 kHz signals for the power supply

14.3.6 INTERRUPTS

There are 2 interrupts used:

INT2:	DUART channel 0 interrupt
INT5:	Early warning from the power supply

14.3.7 SYNCHRONOUS SERIAL UNIT

The synchronous serial port is connected to the A/D converter. The signals used are as follows:

STXCLK:	synchronous transmit clock
SRXCLK:	synchronous receive clock
SSIOTX:	synchronous transmit data
SSIORX:	synchronous receive data

The STXCLK signal is generated in the FPGA circuit each time timer1 initiates a pulse (every 1.25 ms). Sixteen clock pulses are generated by enabling a 25 kHz signal onto the STXCLK line. The A/D is programmed for 16 bit transfers and when the A/D receives the 16^{th} clock, it will activate the EOC signal which turns off the STXCLK signal. The STXCLK signal can also be turned off by setting the ADCS_RESET bit in the Control Register of the FPGA The A/D makes a conversion and passes the data back the next time it receives the STXCLK signal. The SRXCLK signal is connected to the STXCLK and each

time a new conversion is initiated the previous conversion's data is transferred to the 386EX via the SSIORX data line.

14.3.8 ASYNCHRONOUS SERIAL PORT

There are 2 asynchronous UART ports on the 386EX, but only one is used. It is connected to the opto-isolators that connect to the SPO2 unit.

TXD0: asynchronous transmit signal
RXD0: asynchronous receive signal

14.3.9 WATCH DOG TIMER UNIT (WDT)

The watchdog timer unit within the 386EX has one output which goes to the FPGA.

14.4 LNA 386EX CONNECTIONS

LNA 386EX CONNECTIONS

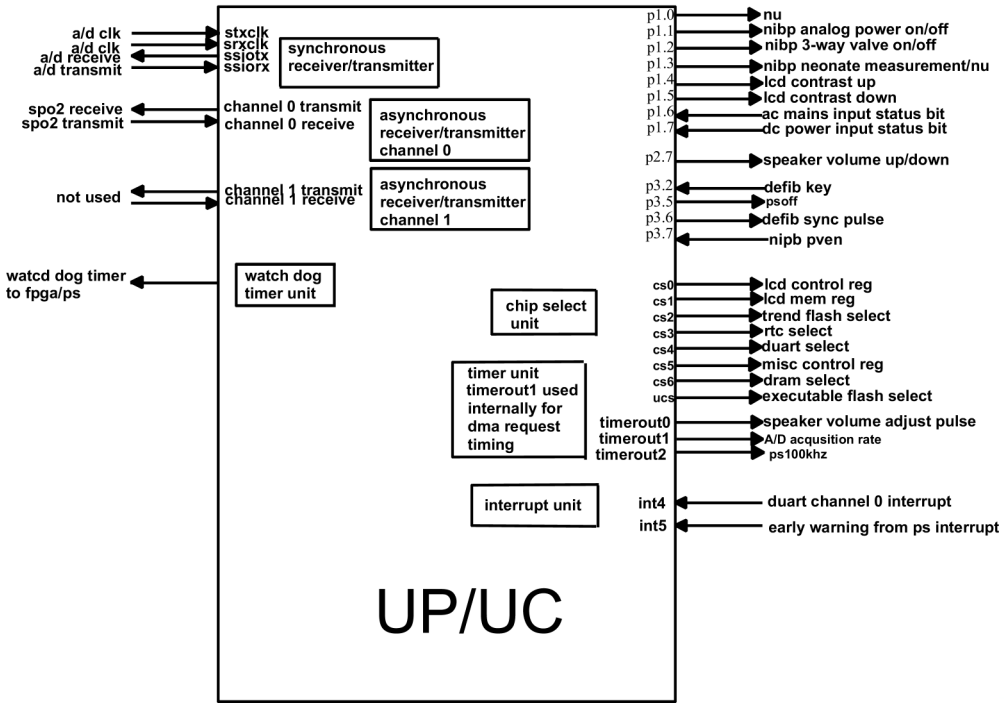

Figure 14-2: LNA 386EX CONNECTIONS

14.5 CPU TIMING SIGNALS

The 386EX runs from a 40mhz crystal oscillator and the main timing is derived from this clock. It is called CLK_40MHZ. Inside the CPU CLK_40MHZ is divided by 2, generating two new clocks, PH1 and PH2. Each T state is made up of one PH1 and one PH2 clock. There are a minimum of 2 T states per cycle. Each wait state is one T state long (50 ns). Therefore, adding wait states is like adds 50 ns on for each wait state.

14.5.1 CPU SIGNALS

Various signals change at various times within a cycle, and the generic timing is shown below. Some of the key signals are ADS#, M/IO#, D/C#, W/R#, WR#, RD#, CS0-CS6#, BLE#, and BHE#. Typical control circuits will look at ADS# at the end of PH2 and make decisions at this time. Refer to the 386EX timing diagrams for a more detailed explanation.

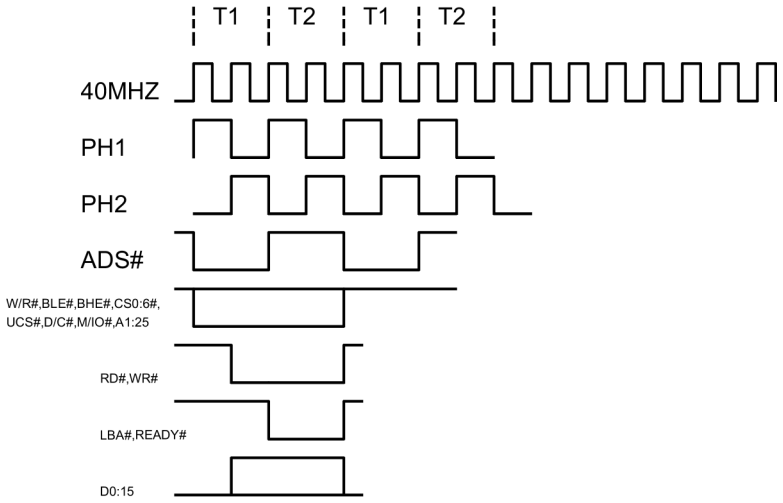

Figure 14-3: CPU Timing Diagram

14.6 DRAM CONTROL

The DRAM control consists of one 1Mx16 EDO DRAM chip, three 74ACT157 address mux chips, address resistors, and the FPGA control circuit.

CS6* (* = # = / a low true signal) has been assigned to the DRAM memory address space, 0-100000 words, or 0-200000 bytes. The CS6* control register in the chip select unit (CSU) must be programmed for 1 WAIT STATE. Since the data bus is 16 bits wide and the DRAM is a x16 part, most transfers will be of the 16 bit variety. However, 8 bit transfers are allowed and we have made provisions for byte addressing. This is done by using the upper and lower CAS signals, UCAS and LCAS.

14.6.1 DRAM SIGNALS

For the DRAM design we must generate 6 signals, RAS#, UCAS#, LCAS#, DRAMOE#, DRAMWR#, and CASADREN. All of these signals are generated in the FPGA from the 386EX signals, ADS#, CS6#, M/IO#, D/C#, WR#, and RD#. Since the CSU is programmed for 1 wait state, the CSU generates the READY# signal which terminates the transfer.

14.6.1.1 DRAM TIMING

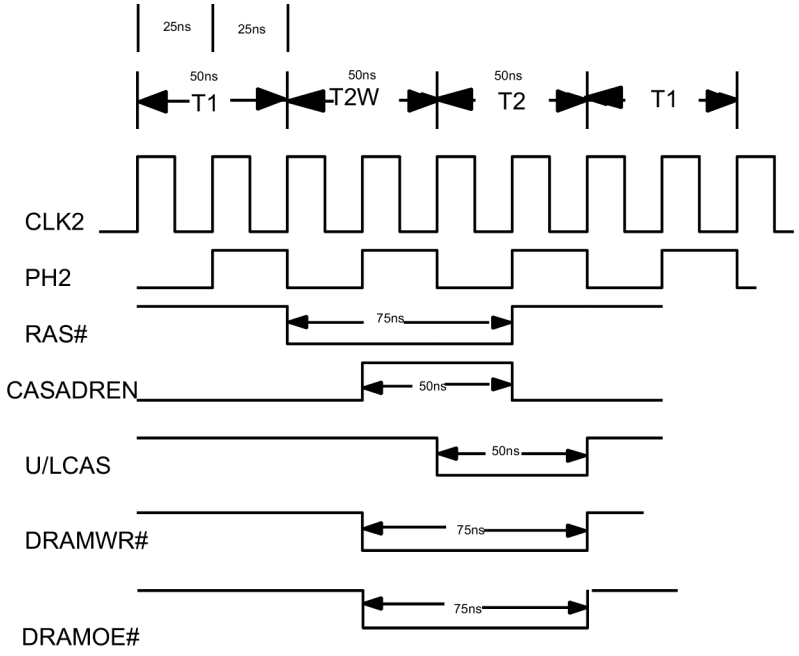

Figure 14-4: DRAM Timing

The DRAM requires 104 ns total time, read/write and precharge for each cycle. There is 1 wait state for each DRAM access and a total of 3 T states which is 150 ns. Since the DRAM minimum access time is 104 ns, we have 46 ns of margin. We are using the Hitachi HM51W18165LTT or equivalent which has a RAS* time of 60 ns, a precharge time of 40 ns, a CAS* time of 10 ns, and a WE* time of 10 ns. The BLE* and BLH* signals are used to select byte oriented reads and writes. There are 2 CAS* lines, which are used to implement the byte writes.

The RAS# and CAS# requirements are shown below.

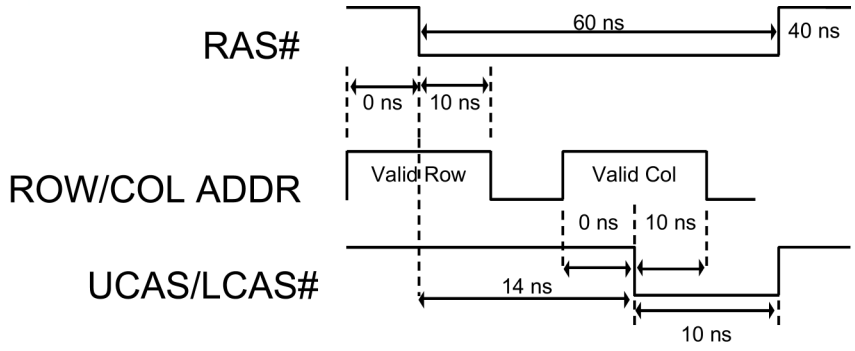

Figure 14-5: RAS# and CAS# Timing

14.6.2 DRAM FPGA CIRCUITS

The DRAM control circuits in the FPGA must decode the various 386EX control signals and generate the DRAM signals. This is done by using CS6# to set a flip flop when ADS# and PH2 are true. When this is true, a flip flop is set, which is output as RAS#. The output of this flip flop is RAS# which is 75 ns long. This signal is generated for all DRAM accesses and refresh. The DRAM output is enabled when either BLE# or BHE# is true, which means a read is occurring. Since the DRAM outputs are bi-directional, we need to disable the DRAMOE# signal if a write is taking place. The WR# signal being false allows DRAMOE# to occur, and if it is true, then the DRAMWR# signal occurs. The BLE# and BHE# signals are also used to generate the UCAS# and LCAS# signals during a read or write operation. Since we are using RAS only for refresh, the CAS signals must be inhibited for refresh.

14.7 FLASH CONTROL

The flash memory and control consists of 2 flash chips, a bootable flash, also called the executable flash, and a trend flash. The control consists of the random logic in the FPGA. The bootable flash is a 512Kx16 Intel) flash with the boot in the top section (T), and is preprogrammed on the data I/O or some other unit with the boot program. The executable program can also be programmed this way or by downloading it to the 386EX via the RS-232 connection. The trend flash consists of Atmel AT29LV256 32kx8 devices which stores the trend data and which writes 64 bytes at a time. It takes 1 wait state for reading the executable, 2 wait states for reading the trend, and 4 wait states to write either of these flashes.

14.7.1 EXECUTABLE FLASH

The executable flash is a word oriented flash, i.e., reading and writing is done on a word basis, and byte reads and writes are not allowed. The trend flash is byte oriented and all reads and writes are done on a byte basis.

The chip select unit has UCS* assigned to the executable flash and CS2* is assigned to the trend flash. Typically, the executable flash is assigned the upper 512 k words, or 1 Megabyte in the system. The word address space is 00000-7FFFF, which is 00000-FFFFF in bytes. This is the upper portion of the space. The trend flash is assigned to the 32 k byte space above the video ram, that is, 84000-8FFFF words, or 11000-14000 bytes. The software, however, has the ability to overlap the trend flash address with the executable flash address. The design gives priority to the trend flash address over the executable flash.

The read cycle time for the executable flash is 90 ns. The write cycle time must be at least 100 ns. Refer to the timing diagrams for the flash for minimum timing parameters.

The executable flash has a delay time of 4 wait states for writing to it.

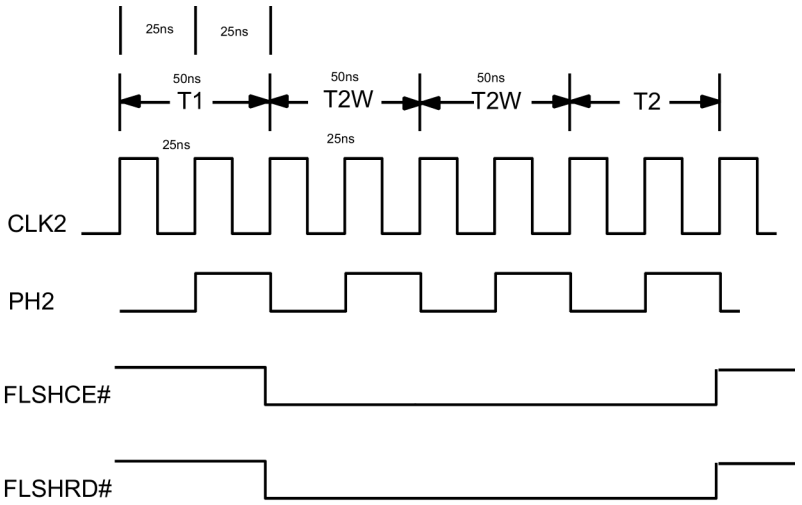

Figure 14-6: Flash Read Timing

In the FPGA control logic, the executable flash chip select is anded with the trend flash chip select such that CS2* must be high, inactive, when addressing the executable flash. This allows the address overlap for the trend flash. The executable flash chip enable FLSH1CE# is generated in the FPGA and then goes to the executable flash. The trend flash is connected directly to CS2# because it has priority over the executable if an overlapping addressing scheme is used. The write pulse width is generated via a state machine to give the proper pulse width

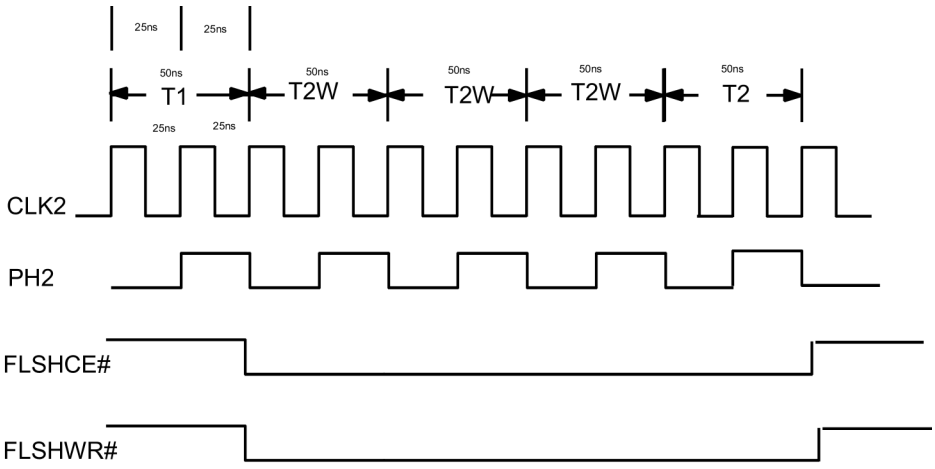

Figure 14-7: Flash Write Timing

14.7.2 FLASH FPGA CONTROL CIRCUIT

The FPGA decodes the boot flash and trend flash select signals and generates the boot flash (FLSH1CE#) signal whenever the trend flash is not being accessed. Since the trend flash address space may overlap the boot flash space, the trend flash has priority.

The flash outputs are enabled for a read cycle. During a write cycle, the data bus inputs data to the flash.

Since the boot flash is for booting up and executing the software program, most accesses to the boot flash are reads. Only when a new program is downloaded will a write to the boot flash occur.

14.7.3 TREND FLASH

The trend flash is different. Its purpose is to store the patients data. It has both read and write accesses occurring at regular intervals. The flash chosen for this purpose interfaces with the 386EX easily, and writing data consists of transferring 64 bytes at a time. The flash takes care of any erasing and writing operations internally. Typical worst case write/erase times for 64 bytes is less than 1 second.

14.8 LCD DISPLAY

The LCD panel is a color 640x3(RGB)x480 pixel TFT (Thin Film Transistor) display. The 1354 drives the display through some translation buffers (74HCT244: U506, U507, U508) because the 1354 operates from the 3.3 volts DC and the LCD display operates from 5 volts DC.

The LCD display is a single panel display constructed of 640x3x480 dots, which equals a total of 921,600 pixels. We wanted 4 bits per pixel, therefor we needed 3,686,400 bits of memory to support the display. A 1MX16 EDO DRAM was chosen because it allowed us to expand to 8 or 16 bits per pixel and it was very inexpensive. The SED1354 supports either a 50 ns or 60 ns access time DRAM. The 60 ns access time is used.

The LCD display interfaces to the S-MOS LCD controller chip, SED1354F0A through some 74HCT244 buffers. This controller chip is connected to the 386EX and one 1MX16 EDO DRAM. The LCD controller has control registers which must be setup by software before writing to the memory and display. It also has configuration inputs that will determine the mode of operation at powerup or reset. The SED1354 is configured in the following. These values could be changed by adding or removing 10k ohm pull-up resistors on the main board. (The 1354 has 100k ohm pull-down resistors built inside the chip.)

Pin Name		**Value of this pin at rising edge of RESET#**
MD[0]	0	16 bit CPU data bus interface
MD[3:1]	011	Generic CPU interface
MD[4]	1	Little Endian
MD[5]	0	Active Low Wait
MD[7:6]	01	Symmetric DRAM
MD[8]	1	General Purpose I/O pins
MD[9]	1	General Purpose Output
MD[10]	0	Active high LCDPWR polarity
MD[15:11]	Not Used	

14.8.1 LCD CONTROL

There are 2 chip selects assigned to the LCD display chip, one for the control registers inside the chip, and one for the display memory space. The chip itself has a state machine controller inside, and generates the necessary signals to store and retrieve data from the memory when requested. It also takes care of driving the LCD display directly, with the data from the display DRAM.

The processor interface consists of the following signals.

CS# is the chip select for the SED1354. It connects directly from the FPGA pin 53 to the SED1345. This signal will go low whenever there is an access by the 386EX to CS0# or CS1#. CS0# relates to the internal registers and CS1# relates the display DRAM.

M/R# is the signal that distinguishes between a memory or register access. When M/R# is low, the 386EX is accessing a register. When M/R# is high, the 386EX is accessing the display memory. This pin is connected directly to the M/IO signal of the 386EX.

RD#, RD/WR#, WE0#, and WE1# are used to read and write to/from the control registers and the display memory. The 2 read signals (RD# and RD/WR#) are connected directly from the FPGA. The 2 write signals (WE0#, and WE1#) are connected directly from the FPGA. When RD# is low, it indicates that Data Bits [7:0] are being read from the 1354. When RD/WR# is low, it indicates that Data Bits [15:8] are being read from the 1354. When both RD# and RD/WR# are low, it indicates that Data Bits [15:0] are being read from the 1354. When WE0# is low, it indicates that Data Bits [7:0] are being written to the 1354. When WE1# is low, it indicates that Data Bits [15:8] are being written to the 1354. When both WE0# and WE1# are low, it indicates that Data Bits [15:0] are being written to the 1354. RD# is generated by "anding" BLE# and RD# of the 386EX, and it comes out of the FPGA pin 59. RD/WR# is generated by "anding" BHE# and RD# of the 386EX, and it comes of the FPGA pin 60. WE0# is generated by "anding" BLE# and WR# of the 386EX, it then gets synchronized with a flip flop. WE0# is on pin 56 of the FPGA. WE1# is generated by "anding" BHE# and WR# of the 386EX, it then gets synchronized with a flip flop. WE1# is on pin 58 of the FPGA.

The CLKI signal is connected to the 40 MHz clock generated by the crystal oscillator X3. This signal provides the pixel clock and the memory clock The 40 MHz frequency allows the software to vary the LCD refresh rate from 80 Hz to 120 Hz

The BUSCLK signal is connected to the 40 MHz clock generated by the crystal oscillator X3. It is the CPU bus clock.

RESET# is connected directly with the RESET# signal from U12 pin 3.

The BS# signal is tied to 3.3 volts DC via a resistor. This pin is suppose to be pulled up in order to operate in Generic CPU mode.

AB0 of the 1354 is connected to BLE# of the 386EX. AB1-AB20 is connected to the address bus of the 386EX.

DB0-DB15 is connected to the bi-directional data bus BD0-BD15.

WAIT# is connected to the FPGA pin 141. When this signal is low, it indicates to the CPU to wait. When this signal goes high data is valid. This signal will be used by the 386EX. The 386EX will insert 2 wait states automatically and end the cycle only when WAIT# returns high.

The above signals are all of the signals used to interface to the 386EX for transferring of data to and from the control registers and the display ram.

There are some general purpose I/O ports that are under software control. They can be programmed as inputs or outputs. Two of these ports are being used (GPIO4 and GPIO5) as outputs and the rest are not being used. If GPIO4 is set, information is displayed left to right. If GPIO4 is cleared, information is displayed right to left. If GPIO5 is set, information is displayed top to bottom. If GPIO5 is cleared, information is displayed bottom to top. The software will program GPIO4 & 5 to be set. The unused ports are pulled-down with 1k ohm resistors on the main board. There is one general purpose output port (pin 106). It is not being used.

14.8.2 LCD DISPLAY RAM

The interface signals for the display RAM are prefaced with the letters VID, which implies video ram. The interface to the display ram (VIDRAM) is defined in the SED1354 Hardware Functional Specification manual and is connected directly to the DRAM.

The LCD display interfaces directly with the SED1354 through the 74HCT244 buffers. The signals used are DRDY, FPFRAME, FPLINE, FPSHIFT, and FPDATA[15:0].

The FPLINE signal is the line pulse, which indicates the start of a line. It is an active low signal. The FPFRAME signal is the frame pulse, which indicates a start-of-frame. It is an active low signal. FPSHIFT is the data shift clock and the LCD display stores the data on the falling edge of this clock. DRDY is the display enable output signal. It indicates when data is ready for each line of video. It is an active high signal. It goes high when data for the line is valid and stays high until the line is finished. FPDATA[15:0] generate the RED, BLUE, GREEN video information and are defined as follows;

FPDATA[15] is Blue bit 1
FPDATA[14] is Blue bit 2
FPDATA[13] is Green bit 0
FPDATA[12] is Green bit 1
FPDATA[11] is Green bit 2
FPDATA[10] is Red bit 1
FPDATA[9] is Red bit 2
FPDATA[8] is Blue bit 3
FPDATA[7] is Blue bit 4
FPDATA[6] is Blue bit 5
FPDATA[5] is Green bit 3
FPDATA[4] is Green bit 4
FPDATA[3] is Green bit 5
FPDATA[2] is Red bit 3
FPDATA[1] is Red bit 4
FPDATA[0] is Red bit 5

The 1354 can only support 64,000 colors, therefore Red bit 0 and Blue bit 0 are not supported and are tied to ground through 1k ohm pull-down resistors (R515 and R516).

14.8.3 LCD AND 386EX INTERFACE

The LCD display chip interfaces directly with the 386EX. When the 386EX initiates a transfer to the 1354F0A, the 386EX generates two wait states and terminates the cycle when the WAIT# signal of the 1354 returns high. This is true for transfers to the 1354F0A's Video Memory or control registers.

14.8.4 LCD CONTRAST CIRCUIT

There is no contrast adjustment for this TFT display. The contrast circuitry is not being used.

Pressing the *Contrast* switch on the front of the NPB-4000C causes the background color to change from a black background to a white background.

14.8.5 BACKLIGHT CIRCUIT

The backlight of the LCD display is a CCFL (cold cathode fluorescent light) and is turned on and off by a digital control bit in the FPGA Control Register. When power is applied it is reset to 0. The backlight requires an AC high voltage which is generated by an inverter, which takes 12 volts DC and generates the AC voltage. When software wants the backlight on it sets this bit and it turns on FET Q1, which completes the circuit to ground and allows the inverter to generate the AC voltage. Resetting this bit breaks the ground connection and inhibits the AC signal to the backlight.

14.9 REAL TIME CLOCK (RTC)

The RTC is a Dallas DS1693 which has the crystal and battery imbedded in the unit. It is a 28 pin DIP package and runs from a 3.3 volt DC supply.

CS3# is assigned to the RTC in the I/O space and the software must assign 14 wait states to this unit.

The timing for the DS1693 is shown below.

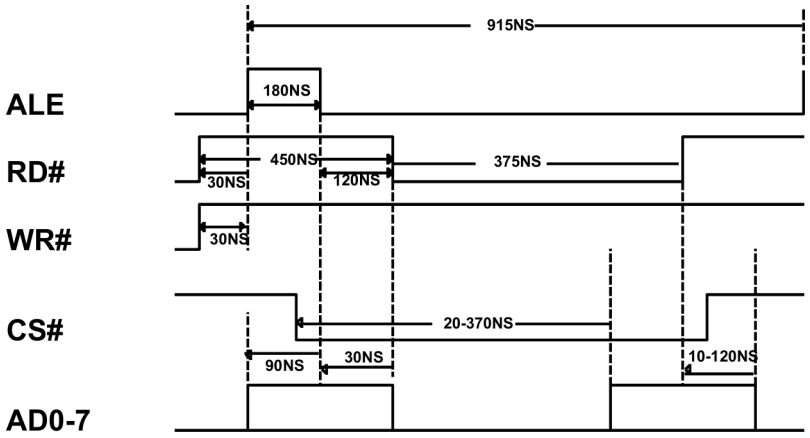

Figure 14-8: DS1693 Timing

The timing for this interface is done in the FPGA. There is a state machine which is clocked at 20 MHz and generates 18 states.

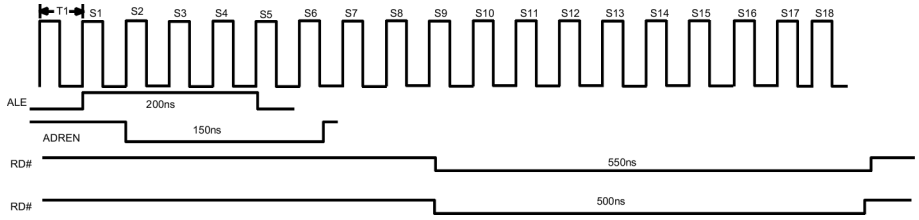

Figure 14-9: Interface Timing

The timing diagram above shows the signals and their relationship to each other.

14.10 DUART CONTROL

The DUART is a Startech ST16C2550CJ44 which consists of 2 UARTs and FIFOS for the read and write portions of each UART. Channel 0 is assigned to the RS-232 port which exits the unit near the AC and DC inputs. Channel 1 is assigned to the recorder. The FIFOS are 16 bytes deep and transfers to/from the DUART would save time if done on 8 or 16 byte boundaries.

Interfacing to the DUART is done by assigning CS4# to the DUART I/O space, with 4 addresses assigned to each UART. The DUART channel 0 is the base address assigned to CS4# and the channel 1 address is the base address + 8 (A3). There are 4 addresses assigned to each UART, 0,1,2,and 3.

Software must program 2 wait states for CS4# and define it as a byte device.

A state machine in the FPGA is used to generate the proper signals for programming the unit.

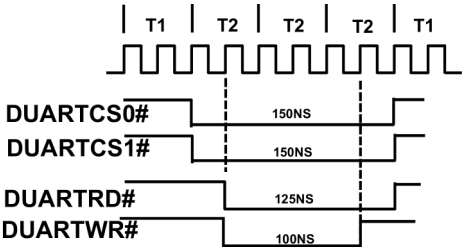

Figure 14-10: DUART Read/Write Timing

14.11 KNOB INTERFACE CONTROL

The knob consists of a rotary knob with a push button switch. The knob is rotated and the cursor on the LCD display moves forward or backward, depending on which way the knob is rotated. When the knob is pushed it must be detected and indicated to the 386EX.

The knob has 2 channels, channel A and channel B. When clockwise rotation occurs, channel A leads channel B and when counter clockwise rotation occurs, channel B leads channel A. The software monitors the knob flip flop and when it is set true the knob has turned. The direction is read by 2 other bits in the status register and the software determines the knob direction. The KNOBINT flip flop in the FPGA is reset by the software when a write to CS5# + A occurs. The knob direction is determined by reading CS5# + A, bits 4 and 5.

The circuit which drives the knob is a 3.3 volt DC circuit, with appropriate resistor values to allow the same current at 3.3 volts through the opto couplers as would have occurred at 5 volts.

14.12 PUSH BUTTON CONTROL

There are 5 push button switches and one knob push button switch. All of these push buttons go to the FPGA control circuit except for the ON/OFF push button, which goes directly to the power supply control circuit. Each of the push button circuits have a debounce resistor and capacitor associated with them and then go to the FPGA. The signals ALRMSIL, NIBPPB, AUDTONVOL, LCDCONTRST, and KNOBPB go to the FPGA where they are “or’ed” together and exit as PBINT. This is read by the software in the status register. The software debounces and detects the length of time the push button is pressed. The software determines which push button was pushed by reading CS5# + c, bits 4-7.

14.13 MISCELLANEOUS CONTROL - CS5#

The NIBP PUMP PWM, NIBP VALVE PWM, SPEAKER FREQUENCY DUTY CYCLE, and a miscellaneous control register are all assigned to the I/O space programmed to CS5#. The addressing scheme is as follows:

CS5#	NIBP PUMP/VALVE PWM 8 bits (R/W)
CS5# + 2	NU
CS5# + 4	SPEAKER HIGH VALUE 8 bits (R/W)
CS5# + 6	SPEAKER LOW VALUE 8 bits (R/W)
CS5# + 8	CONTROL REG. 8 bits (R/W)
CS5# + A	WRITE RESETS KNOB INT/READ PB AND KNOB INT BITS, AND THE KNOB ROTATION DIRECTION BITS
CS5# + C	WRITE WDTEN (WATCH DOG TIMER ENABLE)/READ PUSH BUTTON SWITCHES AND THE KNOB PUSH BUTTON
CS5# + E	WRITE NSCALL (BIT 7) and/or PTRRST (BIT 6)

14.13.1 CS5# NIBP PUMP PWM 8 BITS

The NIBP pump pulse width modulated (PUMP_PWM) signal is generated in the FPGA via an 8 bit register which is clocked at 313 kHz. An 8 bit value is loaded into this register and then the PUMP_PWM_GO bit (bit 0) in the CONTROL REG. is set true and the pump PWM signal begins. The 8 bit register starts counting down and the signal output is low until the counter underflows, at which time it is reloaded with the programmed value. It now counts up, and the signal output goes high until the counter overflows. It is then reloaded and counts down, etc. The PUMP_PWM signal is generated this way until it is shut off by resetting the PUMP_PWM_GO bit in the CONTROL REG.

The NIBP valve pulse width modulated (NIBPCNTLVLV) signal is generated in the FPGA via this same 8 bit register which is clocked at 313 kHz. An 8 bit value is loaded into this register and then the VALVE_PWM_GO bit (bit 1) in the CONTROL REG. is set true and the valve PWM signal begins. The 8 bit register starts counting down and the signal output is low until the counter underflows, at which time it is reloaded with the programmed value. It now counts up, and the signal output goes high until the counter overflows. It is then reloaded and counts down, etc. The NIBPCNTLVLV signal is generated this way until it is shut off by resetting the VALVE_PWM_GO bit in the CONTROL REG.

The same register is used for both PWMs because they are mutually exclusive and software uses only one at a time.

14.13.2 CS5# + 4 SPEAKER HIGH, CS5# + 6 SPEAKER LOW VALUE

The speaker tone frequency is generated using two 8 bit registers, one which is the value for the high portion of the frequency and one value for the low value for the frequency. The frequency range is 200 Hz to 1000 Hz. The 16 bit counter has a count frequency selectable of 78 kHz or 313 kHz. This selection is programmed in the CONTROL REG. using the CLK_FREQ_SEL (bit 2). A 0 selects 156 kHz and a 1 selects 78 kHz. Once the values are loaded and the frequency clock is selected the FREQ_GO bit (bit 3) is set to begin the tone frequency. Software has complete control over the duty cycle of this tone by programming the high and low values and being able to select the clock frequency for the counter. The TONE_OUT signal is low until the low counter overflows and sets the TONE_OUT flip flop high. Now the high counter is enabled and the TONE_OUT signal stays high until the high counter overflows, at which time it goes low and the low counter begins counting. This cycle continues until the FREQ_GO bit is reset to 0.

14.13.3 CS5# + 8 CONTROL REGISTER

This register has 8 programmable bits as follows:

BIT 0: PUMP_PWM_GO
BIT 1: VALVE_PWM_GO
BIT 2: CLK_FREQ_SEL
BIT 3: FREQ_GO
BIT 4: BCK_LITE_ON
BIT 5: FRONT END CLOCK ENABLE
BIT 6: PROGRAM FLASH ENABLE
BIT 7: ADCS RESET

Bits 0-3 were defined in the above paragraphs. Bit 4, BCK_LITE_ON is a bit that turns on the LCD backlight when set to a 1. When powered on this bit is 0 and the backlight is off. To turn on the backlight this bit must be set to a 1.

Bit 5 enables the clock going to the front end transformer, which generates the isolated front end voltages. If the front end should ever go into a base line condition, it is reset by stopping the clock to the transformer and the front end voltages will go to 0. Turning this bit back on powers the front end up and essentially acts as a reset.

Bit 6 enables programming of the boot flash. This would be used if a new executable program were downloaded via the RS-232 channel and stored in the executable flash.

Bit 7 set causes the A/D converter chip select to be set and clears STYXCLK signal. Bit 7 cleared causes the A/D converter chip select to be cleared and starts a conversion sequence.

14.13.4 CS5# + A RESET KNOB INT/READ PUSH BUTTONS

The I/O address of CS5# + 6 has 2 functions associated with it. Writing to this register generates a KNOB_INT_RST signal which resets the knob interrupt flip flops. This would be done by software after a knob interrupt occurs.

The software polls this register every 50 ms and looks to see if the PB_INT bit (bit 6) or the KNOB_INT bit (bit 7) is set true, indicating that a button has been pressed or the knob is being rotated. If either of these bits is true the software must look at bits 3, 4, and 5 to determine which of the knob functions occurred. If the PB_INT is set true, then register C must be read to determine which button was pushed.

Register CS5# + A has the following bit assignments.

BIT 0: Not used
BIT 1: Not used
BIT 2: Not used
BIT 3: Knob push button
BIT 4: Knob channel b rotation
BIT 5: Knob channel a rotation
BIT 6: Push button occurred
BIT 7: Knob rotation occurred

14.13.5 CS5# + C WRITE ENABLES WDT/READ PUSH BUTTONS

After powering up the software must enable the watch dog timer function by writing to this register. The act of writing to CS5#+C automatically sets the WDT flip flop to a one and enables the WDT time out function.

Reading this register gives the push button status, as well as the state of the WDT flip flop.

Register CS5# + C has the following bit assignments.

BIT 0: Not used
BIT 1: Not used
BIT 2: Not used
BIT 3: WDT (watch dog timer enable)
BIT 4: LCD contrast switch
BIT 5: Audio volume switch
BIT 6: NIBP switch
BIT 7: Alarm silence button

14.13.6 CS5# + E WRITE NSCALL/PTRRST/READ PUSH BUTTONS

Writing to this register sets or resets the NURSECALL and PRINTER RESET bits. To set NURSECALL write a 1 to bit 7 and to reset NSCALL write a 0 to bit 7. To reset the printer write a 1 then a 0 to bit 6.

The bit assignments for reading this register are shown below. The bit assignments for writing the NURSECALL and PRINTER RESET are different from the read assignments.

Register CS5# + E has the following bit assignments.

BIT 0: Not used
BIT 1: N Not used
BIT 2: Not used
BIT 3: Not used
BIT 4: Not used
BIT 5: NURSECALL
BIT 6: PRINTER RESET
BIT 7: PRINTER CTS (clear to send)

The NURSECALLL and PRINTER RESET bits are the flip flop outputs programmed by writing to register CS5# + E as explained above.

14.14 SPEAKER

The speaker circuit consists of an 8 ohm speaker driven by a circuit which consists of U26, U27, Q12, Q13, and some discrete resistors and capacitors. U26 is a logarithmic potentiometer which is set by software. Pulses are sent to this potentiometer from a timer in the processor and these pulses turn the volume up and down. A tone is generated by programming the registers in the FPGA and connecting this tone to the potentiometer. The tone's amplitude is modified by the potentiometer and sent to the amplifier U27 which adds a DC offset to the tone and drives transistors Q12 and Q13, which generates a 12 volt signal. This signal goes to a 3.3 ohm resistor and is then capacitively coupled by a 220 uF capacitor to the speaker.

14.15 NIBP (NON INVASIVE BLOOD PRESSURE) CONTROL

NIBP is a measurement taken by wrapping a blood pressure cuff on the patients arm and automatically inflating the cuff, then deflating the cuff under controlled conditions and monitoring the signals from the pressure transducers connected to the cuff air tubes. Pressure signals are amplified, passed to an A/D converter for conversion to digital format, and then analyzed by the processor software.

14.15.1 NIBP System Overview

The NPB-4000C Non-Invasive Blood Pressure (NIBP) measurement and display operations described in this section include the pneumatics of the inflatable cuff and control valves, the specialized front end NIBP circuitry, some of the μP Memory and Control circuitry, some of the Power System, and specific switches on the Keypad. The major blocks involved from the cuff to the microprocessor are the pump, pressure transducers, control valves, digital control circuits, and the analog detection circuits. The pump is mounted on the Power System assembly and is driven by a pulse-width-modulated (PWM) signal from the Digital Hardware section of the Main Board assembly. That signal is gated by an enabling signal originating in the microprocessor of the section of the Main Board. The pumped air is ducted through tubing and valves mounted on the Main Board and made available at the front end connection to the cuff.

Principle of Measurement
Prior to making blood pressure measurements, the cuff is placed around the arterial location of an upper arm (left or right). The NIBP measurement system is initiated by commands responding to pressing the NIBP switch on the front panel. The cuff is inflated at a rate controlled by the pump excitation current to a pressure above diastolic, at which level the artery is effectively occluded. Then, as the cuff pressure is reduced at constant rate, the pressure transducers provide analog signals to the digital hardware where the are digitized and processed to obtain systolic, diastolic, and mean blood pressure values, as well as the beat rate. The technique for translating the pressure signals into the required measurements makes use of the action of the oscillatory characteristic of the returning arterial pressure. The phenomenon is illustrated in the diagram below.

See Figure 14-11. Systolic pressure is defined as the point at which oscillation increases sharply. As the cuff deflates, oscillation amplitude increases to a maximum, and then decreases. The point of peak oscillation amplitude is the mean arterial pressure. The point at which oscillations cease is defined as the diastolic pressure.

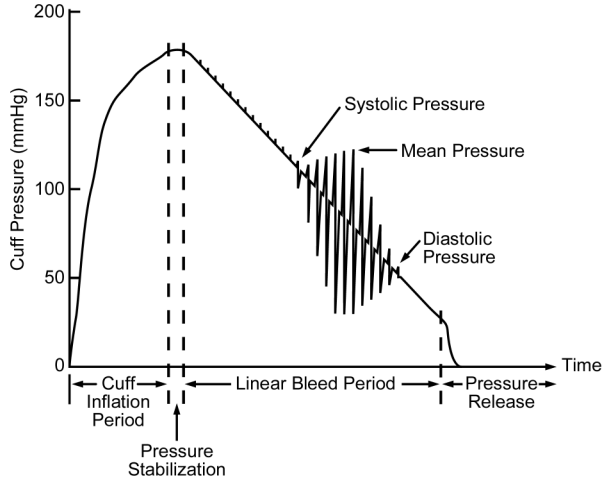

Figure 14-11: Oscillatory Characteristics Diagram

14.15.1.1 The pneumatic assembly

The pneumatic assembly, consisting of the pump, two controlling valves, and tubing to connect the various pneumatic components together are illustrated in the schematic diagram that follows.

See Figure 14-12. The pump output is connected to the cuff and to two valves: a two-way and a three-way valve, as well as to two pressure transducers. Operation of the valves and of the pump control are defined as described in the following text.

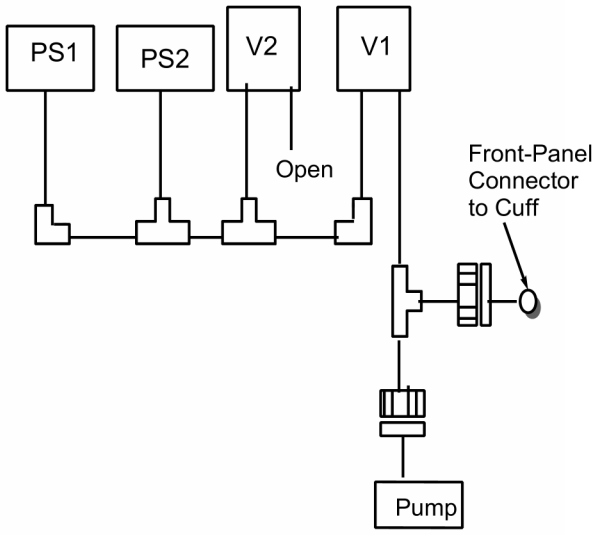

Figure 14-12: Pneumatic Assembly Block Diagram

Control valve V2 is used to control the rate of deflation. The smoothly variable opening of the valve is controlled by the valve excitation current.

3-Way valve V1 is either fully ON or fully OFF. It performs two functions:

1. It dumps the remaining pressure from the cuff at the end of the deflation cycle;

2. It connects the pressure transducers directly to the atmosphere for calibration purposes.

14.15.1.2 NIBP Hardware

The NIBP Analog Control Hardware is highlighted in the block diagram. It includes the front end NIBP circuitry, as well as the pressure transducers and pump.

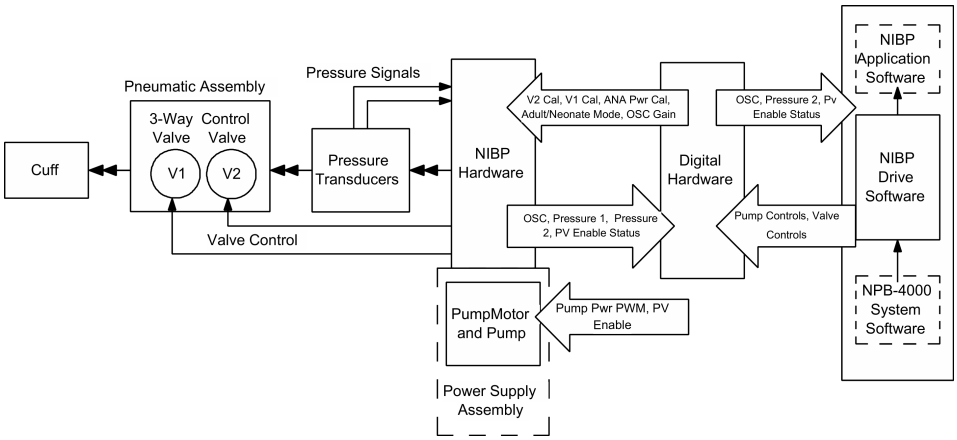

Figure 14-13: NIBP Hardware Block Diagram

14.15.1.2.1 Pressure Transducers

Pressure transducers PS1 and PS2 convert pneumatic pressure levels to voltages in the range from 0.33 volts at 0 mmHg to 4 volts at 300 mmHg. Transducer PS1 is used to sense the main cuff pressure. Transducer PS2 is used as a backup cuff pressure sensor, from which over-pressure warning signals are obtained. Both transducers outputs are smoothed to remove the effects of pumping pulsation. The output of PS1 is identified as signal NIBPPRSR1, while that of PS2 is NIBPPRSR2.

14.15.1.2.2 Filtering the Oscillatory Signal

Amplifiers U16-1 and U16-14, in combination with the lumped resistance and capacitance values of the passive components, form a band pass filter that separates and amplifies the oscillatory signals OSC from the deflating cuff transducer signal NIBPRSR1. Amplifier U16-8 provides hysteresis.

14.15.1.2.3 Power Supplies

Battery power, VBATTP, connected to the board at J3, pins 13 and 14, is regulated in U15 when that component is enabled by the NPANPWR analog power On/Off signal input to U10-4. The regulator accepts a battery voltage of 6 to 8 volts and delivers regulated +5 volts to power the pressure transducers and biasing circuitry for the operational amplifiers.

14.15.1.2.4 Over-Pressure Detector

Pump and Valve drivers are controlled by the NPPVEN pump and valve enable signal that is generated in U16-7 level-detector amplifier circuit. One input to that amplifier is the NIBPRSR2 signal from transducer P2. The other is a value determined by voltage divider R68 and R64, and feedback resistor R61.

The pump and valve drivers are enabled only when cuff pressure is below nominal 330 mmHg for adult mode, and below 165 mmHg for neonatal measurements.

14.15.1.2.5 Pump and Valve Drivers

Three-way valve V1 coil is powered by VPS that is switched in series with the coil through n-channel MOSFET Q10-6. Switching action of Q10-6 is controlled by the input signal NP3WYV, that is gated by the enabling signal NPPVEN at switch U23. VPS is developed from VBATTP through Q11-6 that is also controlled by NPVEN gating transistor Q6. Diode D5 acts to suppress voltage spikes. Resistor R101 insures that Q10-6 will be OFF in case of an open to the input line. The valve is either fully closed, or fully open.

Control valve V2 coil is powered by VBATTP and controlled by switching n-channel MOSFET Q10-7, in series with the coil. Q10-7 is controlled by input signal NIBPCNTLVLV. Pulse width modulation (PWM) of a 5-volt level is used to operate the control valve. No-voltage results in a fully closed valve. As the duty cycle of the PWM is varied from 0 to 100%, the valve changes smoothly from fully closed to fully open. Repetition rate for the PWM is at least 9 kHz. Diode D4 suppresses voltage spikes, and resistor R100 assures that Q10-7 will be OFF if the input line should open.

14.15.1.2.6 NIBP Pump Control

The power supply mechanical assembly holds the blood pressure pump and shield. The power supply contains circuitry that allows logic level control of the pump power from the processor board. For singly-point fault protection, the pump requires two signals (PUMPON and PVENB to activate the pump. PUMPON (when high) turns on FET Q18 that pulls the bottom lead of the motor to ground. PVENB, through level translator Q19, turns on FET Q17 that pulls the top motor lead to VBATT.

When no voltage is present at Q18, the pump is fully OFF. As the duty cycle increases from 0 to 100%, the pump power changes smoothly from full OFF to fully ON. This control technique minimizes overshoot of the targeted pressure. Diode D32 suppresses voltage spikes, while R78 insures that Q18 will be OFF if the line opens. Resistor R77 and capacitor C46 suppress motor brush noise.

14.15.1.3 Digital Signal Processing and Information Display

NPB-4000C software, resident in the microprocessor controller and memory peripherals, include the algorithms needed to process the digitized outputs of the Digital Hardware just described. It also includes the system software that responds to the commands for desired modes of NIBP measurements, display of NIBP values of systolic, diastolic and mean arterial pressure, storing trend data, and for recording/printing of such data, and for initiation and silencing alarms. Details of these functions are contained in the theory of operation of the microprocessor and control circuitry.

14.16 FRONT END INTERFACE

The LNA front end multiplexes analog channels to a linear opto-coupler which is connected to the A/D converter. The A/D converter connects to the transmit and receive ports of the SSIO (Synchronous Serial I/O) unit in the 386EX. Control data is passed to the A/D and the front end via the SSIO signals at the same time

the previous conversion is transferred to the 386EX. The SSIO unit works with the both of the DMA units in the 386EX as well as the timer unit.

The functional operation of the DMA, SSIO, A/D Converter, and the front end is as follows. Software sets up DMA CHANNEL 0 to transfer from DRAM a buffer which contains 16 bit control words. The timer is set up to generate a pulse every 1.25 ms (800 Hz rate). DMA CHANNEL 1 is set up to transfer data from the SSIO receive buffer to a DRAM buffer. The SSIO unit is set up to transmit and receive data when it receives a serial clock. Once set up all of the above circuits work together with the FPGA serial clock circuit to initiate a conversion and transfer the conversions into memory.

The timer output is routed to DMA CHANNEL 0 and the FPGA. The DMA unit transfers a 16 bit control word from DRAM to the SSIO transmit buffer. At the same time the FPGA starts synchronizing to the 25 kHz clock generated internally in the FPGA. The FPGA circuit generates a serial clock which goes to the SSIO clock input and the A/D converter clock input. The SSIO transmit unit starts transmitting the 16 bit control word to the A/D and the front end. The A/D converter receives and interprets the first 8 bits, and ignores the last 8 bits. The front end ignores the first 8 bits and stores the last 8 bits. At the same time that it is receiving the control word, the A/D transmits to the SSIO receive unit the data from the previous conversion. Three things are happening at once. The A/D starts a new conversion after receiving the control word, the A/D transmits to the SSIO the previous conversion's data, and the front end changes it's multiplexer to the new input channel. Since the A/D converter has its own sample and hold, once the conversion begins, the input to the A/D can change without affecting the conversion. Thus, the front end sets up for the next conversion, the A/D starts a conversion, and the A/D also transmits the previous conversion's data. Once the DMA unit receives the new data word from the A/D it transfers it to the DRAM memory.

There is a specific sampling scheme for converting the analog signals. The A/D converter's sampling sequence is programmed by software. The channel selections for the A/D and the front end are contained in the control words transmitted by the SSIO. Since the A/D is a pipelined converter, the A/D channel address sent is for the next conversion, and the front end channel address is for the second conversion. Thus, when a control word is sent, it contains the A/D channel to convert, and the front end channel for the next conversion. The data that gets transferred is for the previous channel. Sampling occurs every 1.25 ms (800 Hz rate), and there is room for 20 samples in a cycle. The samples are repeated every 500 ms.

14.16.1 TIMER/DMA/SSIO INTERFACE

The software sets up TIMER1 to generate an output at an 800 Hz rate (1.25 ms). The timer is routed to DMA CHANNEL 0 which is programmed to transfer a 16 bit control word to the SSIO transmit holding buffer. The SSIO transmits this word to the A/D and the front end. The A/D stores the first 8 bits and the front end stores the last 8 bits. At the same time the A/D transfers to the SSIO receive buffer the previous conversions data. When the SSIO receive buffer becomes full, it starts DMA CHANNEL 1, which transfers the data word to memory from the SSIO receive buffer. This process continues indefinitely.

The control words sent to the A/D converter contain the A/D multiplexer channel to convert, the data length, data format, and whether the conversion is a unipolar or bipolar conversion.

The first bit transferred out the SSIO transmit line is the most significant bit, bit 15. The A/D takes bits 15-8 and the front end takes bits 7-0. Bit definitions are as follows.

BIT 16-12:	A/D MUX CHANNEL SELECT
BIT 11-10:	A/D DATA LENGTH
BIT 9:	A/D DATA FORMAT
BIT 8:	UNIPOLAR/BIPOLAR

Once the A/D reads these 8 bits, a conversion starts.

BIT 7-5:	FRONT END MUX CHANNEL SELECT
BIT 4-3:	LEAD SELECT
BIT 2:	0.5 HZ FILTER SELECT
BIT 1:	BASELINE RESET
BIT 0:	PARITY

Once these 8 bits are strobed into the front end serial shift register, a load pulse is generated which transfers these bits to the output register in the shift register and these bits now become effective.

14.17 DIGITAL SCHEMATIC

These schematics include all of the above circuits and some additional circuits which need explanations. The schematic contains the following chips:

386EXMP	microcontroller
42MX09	programmable device with the control circuits
LCD CONTROLLER 1354F0A LCD	display control chip
74HCT244	buffer chips for the signals from the LCD controller to the display itself
74LVC16245	data bus buffer to interface the 386EX to the other chips
RTC DS1693	real time clock with 64 bytes of battery backed ram and on board crystal
74LVC541	mux for the address/data to the RTC
DUART	dual uart for the RS232 and recorder
MAX211E	RS232 interface chip with 15kv ESD
DISPLAY RAM	1MX16 EDO DRAM for the LCD display
DRAM	1Mx16 EDO dynamic ram memory
74ACT157	address mux for the DRAM
BOOT FLASH	bootable/executable flash memory
TREND FLASH	flash memory for storing trend data
OSCILLATOR	40mhz oscillator to generate CLK2

The schematics contains the NIBP circuits, the speaker circuits, the battery voltage and temperature input circuits, the push button interface circuit, and the backlight interface connector circuit. The 50 pin connector connects to the recorder, RS-232 connector, the power supply connector, the DEFIB connector, and the speaker.

The speaker circuit consists of a software programmable digital potentiometer chip, U28, which is a Dallas DS1666s-10. The software sets the tone frequency by setting the high register with a value, the low register with a value, then programming the digital potentiometer up/down according to the timing specified in the requirement specification.

14.17.1 FPGA THEORY OF OPERATION

The Actel FPGA is a 3.3 volt, 9000 gate device which contains miscellaneous control and glue logic for the NPB-4000C. It is packaged in a 176 pin TQFP.

The FPGA contains the following control circuits.

1. DRAM control
2. FLASH control
3. PUSH BUTTON detect
4. RESET/CLOCK PHASE control
5. BIDIRECTIONAL DATA BUFFER control
6. CONTROL REGISTER control
7. READY/ control
8. RTC/DUART state machine/control
9. READ-BACK multiplexer
10. PUMP/VALVE PWM
11. CONTRAST PWM (not used)
12. SPEAKER FREQUENCY generator
13. KNOB detect
14. POWER SUPPLY SYNC ALARM control
15. A/D CONVERTER SERIAL CLOCK control
16. LCD control

14.17.2 DRAM CONTROL CIRCUIT

The DRAM control circuits consist of a small state machine to generate RAS/, LCAS/, UCAS/,DRAMOE/, WRITE/, CASADREN/, FDRRD, and ENDTABFR. The process of reading, writing, and refreshing the DRAM is controlled by these circuits. Each portion of the circuit is described below.

RAS/ (Row Address Strobe) is a 75 ns signal which strobes the row address into the DRAM. Next, a 50 ns signal called LCAS/ (Lower Column Address Strobe) and/or UCAS/ (Upper Column Address Strobe) is/are generated which strobes the column address into the DRAM. Once RAS/ and LCAS/ and/or UCAS/ have occurred, either a read of the DRAM takes place if DRAMOE/ is true, or a write to the DRAM takes place if WRITE/ is true. Only one of these last 2 signals can be true at one time. 25 ns before CAS/ occurs, CASADREN is generated. When this signal is high the row address is enabled to the DRAM and when it is low the column address is enabled to the DRAM. The signal ENDTABFR is a low true signal and enables the data bus buffer on the Mother Board (D5-18055) to transfer data to or from the 386EX.

14.17.3 RAS/ CONTROL CIRCUIT

The RAS/ control circuit consists of 5 flip flops called STARTFF, DRAMINFF, RAS1FF, RAS2FF, and RAS3FF. The ADS/ signal from the 386EX is anded with the CLK_PH2 signal and then goes to the IDE/ input of the DRAMINFF. CS6/ (DRAM chip select) goes to the D input. It is clocked into the flip flop on the rising edge of the IOCLOCK signal at the end of the T1 state (which is the same as the beginning of the T2 state). At the same time the STARTFF is conditioned to get set every time CLK_PH2 and ADS/ occur. This signifies the beginning of a cycle because ADS/ is only true at the beginning of a new cycle. Once these 2 flip flops are set RAS/ is generated and goes out of the FPGA on pin 138. CASADREN is low and enables the row address to the DRAM. On the next 3 consecutive CLK_40MHZ rising edges, RAS1FF is set low, then RAS2FF is set low, and finally RAS3FF is set low. This takes 75 ns, and when RAS3FF is set low it disables the RASAND gate and turns off RAS/ (RAS/ goes high).

The STARTFF had to be added because if an idle state occurs after a DRAM read the RAS state machine does not turn off properly and it will not pick up the next DRAM read if it follows the idle state. What was happening was as follows. The DRAMINFF is set at the beginning of the T2 state of a valid DRAM read cycle. The RAS1FF is set 25 ns later, the RAS2FF is set 25 ns after that, and the RAS3FF is set 25 ns after that. It takes another 75 ns for each of these flip flops to turn off and this extends into the first T state of the next cycle. If it is a valid cycle everything is OK. If, however, it is an idle state, then the state machine just continues to turn back on because CS6/ remains low during the idle state even though it's not doing a DRAM read. Since the state machine thinks it is back on, it does a DRAM read cycle, but it is out of sync with the actual next DRAM read. The idle state is only one T state long (50 ns) and the easiest solution at the time was to put in the STARTFF which turns on only when ADS/ is true which can only occur at the beginning of a valid cycle and not when an idle state occurs. The STARTFF turns off when the READY/ signal occurs which happens at the end of each cycle. This gives a definitive start and stop for each valid cycle.

14.17.3.1 UCAS/ and LCAS/ CONTROL CIRCUITS

25 ns after RAS/ goes low, RAS1FF/ goes low and CASADREN goes low, enabling the column address to the DRAM. 25ns later RAS2FF/ is set low, and is conditioned with BLEB/, RAS1/, and LCD_MEM_SEL/ to generate LCAS/. Substituting BHEB/ for BLEB/ and conditioning with the same signals, UCAS/ is generated. The DRAM is separated into upper and lower portions and require separate CAS signals, hence the UCAS/ and LCAS/ signals. BLEB and BHEB are low byte and high byte enable signals from the 386EX. LCD_MEM_SEL/ is part of the conditioning because software requested that the display memory might be overlaid with the DRAM memory and, therefore, it has priority.

14.17.3.2 DRAMOE/ CONTROL CIRCUIT

The DRAMOE/ signal enables the output drivers in the DRAM which is activated on a read of the DRAM memory. DRAMOE/ is generated from RAS1/, BLEORBHE, WRB/, and LCD_MEM_SEL/. The RAS1/ must be low, indicating that a DRAM access is beginning. The BLEORBHE is high (true) and indicates that a valid read is occurring. The WRB/ must be high indicating that a write is not taking place, and LCD_MEM_SEL/ is high indicating that the memory location is mapped to DRAM and not LCD memory.

14.17.3.3 CASADREN SIGNAL

The CASADREN signal is a signal which enables the row address and column address to the DRAM when RAS/ and CAS/ are generated. This signal is high and enables the row address when RAS/ goes low and remains high until RAS1/ goes low at which time CASADREN goes low, enabling the column address. This occurs 25 ns before LCAS/ or UCAS/ goes low. It is connected to the RAS1/ signal and stays low for 75 ns.

14.17.3.4 WRITE SIGNAL

The WRITE/ signal is generated for writing to DRAM, FLASH, RTC, and the DUART. Writing to the DRAM occurs when RAS1/ is true, WRB/ is true, LCD_MEM_SEL/ is false, and D_CB is high, indicating a data operation. As a note, a WRITE/ must be generated in glue logic because various memory and peripheral chips require a hold time when writing data to it. The 386EX turns the WR/ signal off at the end of the last T2 state of a cycle. When this happens, the data bus buffer is also turned off and the data lines go into a tri-state condition. This can happen rather quickly, (less then 5 ns) and cannot guarantee a decent hold time for the data being written.

14.17.3.5 ENDTABFR SIGNAL

The signal ENDTABFR is a low true signal and enables the data bus buffer on the Mother Board (D5-18055) to transfer data to or from the 386EX. It powers up in the high state and is set low when ADSB/ goes low, which signifies that a new cycle is beginning. This is true for all transfers except if the RTC is selected. If the RTC is selected then the signal doesn't go low until state 9 of the RTC state machine. This is ensured by jamming the D input with a high signal generated by the anding of RTC_SEL low and the state machine having not reached state 8. When ENDTABFR is low, it is set high again when the READY/ signal goes low, signifying the end of a cycle. The RTC has a multiplexed address/data bus and requires that the data bus buffer be tri-stated when the address is enabled to the RTC chip.

14.17.4 CONTROL REGISTER DECODE

The CONTROL REGISTER decoder is a 1 of 8 decoder which decodes the register addresses for the 8 control registers in the FPGA. The decoder generates a high going pulse coincident with WRB/ on 1 of the 8 output signal lines. The register addresses are as follows:

1. LOAD NIBP PUMP PWM — ADDRESS 300 HEX
2. LOAD CONTRAST PWM — ADDRESS 302 HEX, NOT USED
3. LOAD SPEAKER HIGH — ADDRESS 304 HEX
4. LOAD SPEAKER LOW — ADDRESS 306 HEX
5. LOAD CONTROL REG — ADDRESS 308 HEX
6. RESET KNOB INTERRUPT — ADDRESS 30A HEX
7. ENABLE WATCH DOG TIMER — ADDRESS 30C HEX
8. LOAD CONTROL REG 2

The function of each of these registers is explained later.

14.17.5 PUSH BUTTON INTERRUPT

When a membrane switch is pressed, a low true signal occurs. All of the membrane switches are or'ed together to generate the PBINTPD signal which is read via the status register. This signal also comes out on pin 81 of the FPGA for testing purposes only. It does not go the 386EX interrupt inputs. The software polls the status register at a known rate and checks to see if this bit is set.

14.17.6 WATCH DOG TIMER ENABLE

The WDT output from the 386EX is anded with a 50 kHz signal which is derived from the 100 kHz output of timer 2 of the 386EX. When powering up the WDT is not in the correct mode of operation until the software programs it. Therefore, to prevent the power supply from shutting down prematurely, the WDTENFF must be set high after the WDT has been programmed. Writing to address 30C automatically sets this bit high and enables the WDT function.

14.17.7 REGISTER 30E

This register has 2 bits, NSCALL (nurse call) and PTRRST (printer reset). Each of these bits can be set high or low by programming the bit 6 for the PTRRST signal and bit 7 for the NSCALL signal. The NSCALL signal goes out on pin 123 and PTRRST goes out on pin 151.

14.17.8 FLASH CHIP ENABLE

The EXECUTABLE FLASH chip is assigned to UCS (upper chip select) and the TREND FLASH is assigned to CS2. Software requested that they be able to map the TREND FLASH in the EXECUTABLE FLASH address space. To accomplish this the TREND FLASH selection has priority over the EXECUTABLE FLASH. Thus, the EXECUTABLE FLASH chip select must be conditioned with the TREND FLASH chip select. This is done by anding BOOTFLSHSEL/ low with TRND_FLSH_SEL/ high and M_IOB/ high. The FLSH1CE/ low gets generated whenever the BOOT FLASH is being addressed and the TREND FLASH is not being addressed.

14.17.9 FLASH WRITE STATE MACHINE

The FLASH write state machine consists of 5 flip flops and is set into action when CS2/ or UCS/ is low, CLK_PH1 is high (which indicates the first phase of the T2 state), WRB/ is low, and BLEORBHE is high indicating a byte or word transfer. The FLSHWRFF1 signal is set true at the midpoint of T2, which generates FLASHWRT and WRITE/ on pin 2. The state machine flip flops are clocked on CLK_PH1 which occurs at the beginning of each T2 state. There are 4 flip flops which gives a 200 ns time, and the FLSHWRT signal gets turned off at the mid point of the last T2 state, generating a total WRITE/ low pulse of 250 ns. Minimum for either FLASH is 200 ns.

14.17.10 RESET/CLOCK PHASE CLOCK CIRCUITS

When power is turned on, a reset signal is enters on pin 104. The RESETFF is set true on the next CLK_40MHZ rising clock edge and RESET exits on pin 63. This is the master reset signal for the whole board and the 386EX. At the same time it is required to make sure that the control circuits are in sync with the 386EX, and this is done by generating our own phase 1 (CLK_PH1) and phase 2 (CLK_PH2) signals. The CLK_PH1 signal starts as soon as RESET goes low, and CLK_PH2 always follows CLK_PH1 and is the inverse of CLK_PH1. These clocks are 50 percent duty cycle clocks running at 20 MHz (50 ns period). Each T state of the processor is composed of 2 phases or clock states, first CLK_PH1, then CLK_PH2, and is 50 ns long.

14.17.11 READY/ CIRCUIT

The READY/ circuit is complicated by the fact that either the processor or an external peripheral can generate the READY/ signal. There are 2 conditions under which an external READY/ signal can be generated. First was any access to the LCD controller or memory, and second, when a HALT instruction is executed. The software programs 2 wait states for any access to the LCD controller and each access is terminated after the WAIT# signal from the 1354 returns high. The WAIT# signal is connected to pin 141 of the FPGA. The other remaining circuit requiring and external READY/ is when a HALT instruction is executed. The HALT AND gate ands D_CB/ low, M_IOB/high, and W_RB/ high to generate a READY/. The HALT READY/ and LCD WAIT# are connected through a multiplexer which connects to the 386 READY/. This READY/ signal comes out on pin 47 of the FPGA.

14.17.12 MICELLANEOUS CLOCK CIRCUITS

The master clock from the 40 MHz oscillator enters the FPGA on pin 154 and 75. The CLK2_40MHZ is the 40 MHz internal clock for the FPGA. A 20 MHz clock enters the FPGA on pin 158, this signal is generated by the 386EX. This signal called PHI1-FPGA will be used in the LCD control circuit.

14.17.13 RTC/DUART STATE MACHINE

Interfacing to the DUART and RTC requires slowing down the signals. A 20 state machine is implemented to interface to these circuits. The state machine always starts up when ADSB/ is low and CLK_PH1 is high. The RTC1AFF is set high on the rising edge of the master clock, CLK2_40MHZ. If the RTC or DUART is not selected, the state machine is reset on the next CLK2_40MHZ. The first 2 flip flops of the state machine are clocked on the CLK2_40MHZ rising edge, while the remaining flops are clocked on the rising edge of CLK_PH1, which occurs at the beginning of each state. The time between the rising edges of this clock is 50 ns. The total time for the state machine is 1000 ns (1 us). This is required for the RTC, but the DUART only requires 4 states, 200 ns. The software programs the CS4 (DUART) for 2 wait state and the RTC for 18 wait states.

14.17.14 RTC CONTROL

The RTC control signals consist of READ_RTC, WRITE_RTC, RTC_ADREN/, and RTC_ALE. These are all generated from the state machine cycles. The RTC has a multiplexed address/data bus, and, therefore, requires that the bi-directional data bus be tri-stated while the address is enabled to the RTC. The ENDTABFR signal is disabled high if the RTC is selected. It is jammed high by the ENDTARTCAND gate which ands RTC_SEL/ low and RTCS8 low. ENDTABFR goes low at the start of state 9 by anding RTCS9 low and RTCS8 high. During the time ENDTABFR is high, the address is enabled by RTC_ADREN/, which is generated when RTCS2 is high and while RTCS8 is low. At this same time RTC_ALE is generated between states 1 and 5, latching the address into the RTC. When state 9 is reached, either a read or write happens, depending on the state of the WR/ and RD/ signals. The READ_RTC is generated between the states 9 and 20, while WRITE_RTC is generated between the states of 9 and 19. The READ_RTC generates FDRRD/ on pin 46. The WRITE_RTC generates WRITE/ on pin 2.

In review, the RTC control has to enable the address to the RTC and generate the RTC_ALE signal to latch the address. Next, the data buffer must be enabled in the proper direction and the read or write signals generated.

14.17.15 DUART CONTROL

The DUART has 2 UART channels within one chip, and the chip select (CS4) is used for both. The base address is used to program UART channel 0, and the base address + 80 hex is used to program UART channel 1. This decoding is done under the DUART control section and the 2 chip selects (DURT0_CS and DURT1_CS). The software programs 2 wait states for the DUART. The READ_DUART signal is generated from the state machine states 1 to 3, shutting off in state 4. This gives a 150 ns read pulse. The write pulse is generated from states 1 to2, shutting off in state 3, generating a 100 ns write pulse. This gives a 50 ns hold time on the data to the DUART.

14.17.16 FREQUENCY GENERATOR

The master clock in, generates 2 internal signals, CLK_PH1 and CLK_PH2, both of which are 20 MHz clocks 180 degrees out of phase with each other. The CLK_PH1 is divided down into 10 MHz, 5 MHz, 2.5 MHz, 1.25 MHz, 525 kHz, 313 kHz, 156 kHz, and 78 kHz. The 10 MHz is output on pin 139 and goes to the DUART controller as its master clock. 313 kHz is used by the NIBP PWM circuits. The 156 kHz and 78 kHz are used by the speaker frequency generating circuit.

14.17.17 LCD CONTROL

The LCD CONTROL circuit generates the control signals for the SED1354, they are RD_WR/, RD/, WR0/, WR1/, and CS/.

The RD/ is generated by anding BLEB/ with RDB/. The output signal is called LCD_LRD/. This signal comes from pin 59 of the FPGA and goes to pin 7 of the 1354.

The RD_WR/ is generated by anding BHEB/ with RD/. The output signal is called LCD_URD/. This signal comes from pin 60 of the FPGA and goes to pin 10 of the 1354.

The WR0/ is generated by an AND gate and a flip flop. The AND gate is "anding" BLEB/ with WRB/. The flip flop is used to delay the WR0/. The reason for the delay is to ensure that data out of the 386 is valid and to meet the maximum delay from WR0/ low to data valid of the 1354. The flip flop will become cleared when ADS/ goes low for the start of the next cycle. The output signal is called LCD_LWR/. This signal comes from pin 56 of the FPGA and goes to pin 8 of the 1354.

The WR1/ is generated by an AND gate and a flip flop. The AND gate is "anding" BHEB/ with WRB/. The flip flop is used to delay the WR1/. The reason for the delay is to ensure that data out of the 386 is valid and to meet the maximum delay from WR0/ low to data valid of the 1354. The flip flop will become cleared when ADS/ goes low for the start of the next cycle. The output signal is called LCD_UWR/. This signal comes from pin 58 of the FPGA and goes to pin 9 of the 1354.

CS/ is essentially generated by "or'ing" LCD_CNTL_SEL/ with LCD_MEM_SEL/. The First flip flop will become set when ADS/ and PHI1_FPGA are both low to indicate the start of a cycle The Second flip flop will get set when LCD_CNTL_SEL/ or LCD_MEM_SEL/ is low and the First flip flop is set. The Third flip flop will get set 25 ns after the Second. The reason for the third flip flop is to meet the minimum timing from WE0/ or WE1/ low to CS/ low of the 1354. The flip flops will stay latched until LCD_CNTL_SEL and LCD_MEM_SEL/ are both high or if ADS/ goes low. The output signal is called LCD_CS/. It comes from the FPGA pin 53 and goes to pin 4 of the 1354.

14.17.18 READ BACK MULTIPLEXER

A read back multiplexer allows the software to read back programmed and status signals from the FPGA. Register assignments are as follows:

1.	PUMP/VALVE PWM	300 HEX
2.	CONTRAST PWM	302 HEX, not used
3.	SPEAKER HIGH VALUE	304 HEX
4.	SPEAKER LOW VALUE	306 HEX
5.	CONTROL REG	308 HEX
6.	PUSH BUTTON STATUS	30A HEX
7.	KNOB/MISC STATUS	30C HEX
8.	MISC STATUS	30E HEX

14.17.19 NIBP PUMP/VALVE PWM CONTROL

This circuit consists of an 8 bit holding register and an 8 bit up/down counter. This circuit is first used to control the NIBP pump by generating a pulse width modulated signal which drives the pump on the POWER SUPPLY board. After the pump has inflated the cuff, this same circuit is used to control opening the valve to let the air out of the cuff. The pump PWM signal exits on pin 4 and the valve PWM exits on pin 132. The enable for these 2 output buffers are programmed in the control register and are mutually exclusive.

The software loads a value into the 8 bit holding register. The counter is clocked by a 313 kHz clock and on all the time. When the counter overflows, the value in the holding register is loaded into the counter synchronously with the 313 kHz clock. The counter operates as a count up then count down circuit, always generating the same frequency, but with different duty cycles. Once a value is loaded into the counter, the counter counts up until it overflows. If PUMP_PWM_GO is true, then the PUMP_PWM_FF is output on pin 3. When the counter overflows, the PUMP_PWM_FF changes state, and the counter is reloaded with the holding register's value. Now the counter counts down until it underflows, at which time, the flip flop changes state, the holding register's value is reloaded and counting continues in the up direction. Since the same value is loaded each time, the total time for a count up and a count down is 313 kHz divided by 255, and, therefore, the signal frequency remains the same. The duty cycle changes as the software programs the holding register, thus allowing for a fully OFF to a fully ON signal with intermediate steps at a 3.2 us resolution.

14.17.20 SPEAKER HIGH AND LOW CONTROL

The speaker requires tones from about 300 Hz to 1 kHz with a 55 percent duty cycle. In order to give software full control over both the frequency and duty cycle, there are 2 software programmable 8 bit up counters, one for generating the low portion of the TONE_OUT and one for generating the high portion. The TONE_OUT flip flop is jammed reset when the FREQ_GO bit in the control register is low. This enables the SPEAKER LOW counter. The software programs the high and low values into the respective holding registers, then sets the FREQ_GO bit. The TONE_OUT on pin 93 is low, and remains low until the SPEAKER LOW counter overflows, which sets the TONE_OUT high and loads the SPEAKER HIGH counter. This counter now increments until it overflows, which now sets the TONE_OUT signal low and reloads the SPEAKER LOW counter. This process continues until the software turns off the TONE_OUT signal by resetting the FREQ_GO bit in the control register.

14.17.21 CONTROL REGISTER

The control register is an 8 bit register with miscellaneous programmable control bits. These 8 bits are programmable and can be read back via the read back multiplexer.

14.17.21.1 PUMP_PWM_GO and VALVE_PWM_GO BITS

The PUMP_PWM_GO is bit 0 and VALVE_PWM_GO is bit 1. These bits have been mentioned above and are used to control the pump control signal for inflating the cuff and the valve control signal for deflating the cuff.

14.17.21.2 CLK_FREQ_SEL CONTROL BIT

Bit 2 is the CLK_FREQ_SEL bit which selects the clock frequency for the speaker counting registers. When low 156 kHz is selected and when high 313 kHz is selected. The 156 kHz is required so we can generate the low tones with the two 8 bit counters.

14.17.21.3 FREQ_GO BIT

The FREQ_GO is bit 3 and is used to control the TONE_OUT signal to the speaker. Setting this bit to a high enables the TONE_OUT and setting it low, disables the TONE_OUT.

14.17.21.4 BCK_LITE_ON

This is bit 4 and is used to turn the LCD display CCF (Cold Cathode Fluorescent) backlight ON and OFF. Setting this bit high turns the backlight on and setting this bit low turns the backlight off.

14.17.21.5 FE_CLK_EN BIT

Bit 5 is the FE_CLK_EN which stands for the front end clock enable bit. This bit enables the 200 kHz signal to the front end power supply transformer. The software has control over the front end power supply via this bit. The major reason for having this bit is to reset the front end by turning the power OFF, then ON again via this bit.

14.17.21.6 PROG_EN BIT

Bit 6 is the program enable bit for reprogramming or storing data in the executable FLASH. This bit when high enables the +3.3 volts DC onto the programming bit of the FLASH. This allows data to be written into the FLASH by writing to the FLASH.

14.17.21.7 ADCS_RESET BIT

This bit when high resets the A/D converter and clears the STYXCLK signal. It holds the A/D converter in reset state until this bit is set low. This bit exits the FPGA via pin 162.

14.17.22 STXCLK and ADCS/ CIRCUITS

The A/D converter has a synchronous serial interface (SSIO) to the 386EX. The 3 signals are transmit data, receive data, and clock. When the SSIO port in the 386EX is programmed and activated, it operates in an unusual manner. If new data is not ready after a transmission, the serial unit will transmit the same data over again. The solution is to generate the synchronous serial clock in the FPGA rather than the 386EX SSIO unit. The TIMER0'S output is routed to the FPGA on pin 95 and enables a 25 kHz clock which goes out on pin 134. This is the master synchronous serial clock and is routed to the A/D converter and the 386EX SSIO unit. The 386EX SSIO unit is programmed as a slave for the serial clock and thus when it receives the serial clock from the FPGA it starts enabling data onto the transmit line, and receives data on the receive line. The A/D converter receives 16 clocks and then asserts its EOC signal which comes in on pin 43. This turns off the serial clock and it doesn't turn on again until the next tick from the timer. (The serial clock can also be turned off by setting the ADCS_RESET bit in the CONTROL Register of the FPGA.) This same timer tick is routed to the 386EX DMA unit and a new piece of data is transferred to the SSIO unit in a waiting buffer. After the present data is transmitted, the new data is loaded into the transmit register and is ready for transmission on the next timer tick. This solves the problem of the SSIO unit retransmitting data.

14.17.23 SYNC_ALARM CIRCUIT

The power supply board requires a 50 kHz signal to generate the various voltages in the system. A 100 kHz, 50 percent duty cycle signal is programmed in the 386EX TIMER 1 unit. It enters the FPGA on pin 119 and is divided by 2 to get 50 kHz. This is anded with the WDT (pin 62) signal from the 386EX. The WDTDETFF is held reset until enabled by WDTEN. If the WDT should time out the WDTDETFF flip flop is set and disables the 50 kHz SYNC_ALARM signal from going to the power supply, which will generate an EARLEY WARNING signal to the 386EX and then shut off power to the main board.

14.17.24 FE_CLK_100KHZ

This circuit feeds the 100 kHz clock from TIMER1 to pin 129 to the front end for its power supply. It is enabled by FE_CLK_EN from the CONTROL REGISTER as described earlier. The 100 kHz is not divided, the TIMER1 counter must be set into a mode which produces a 50 percent duty cycle square wave.

14.17.25 KNOB ROTATION DETECT

The rotating knob on the front of the unit has an optical interface. Five volts are supplied to it and it generates 2 signal channels (A and B) which are input to the FPGA on pins 163 and 164. When the knob rotates clockwise the square wave on CHANNEL A leads the square wave on CHANNEL B by 90 degrees. When rotating counter clockwise, CHANNEL B leads CHANNEL A by 90 degrees. This circuit exclusively ors the channels and generates an edge each time a channel input changes state. One flip flop is set on the rising edge and another is set on the trailing edge. These 2 flip flops are or'ed together and exit on pin 100, which is for debugging purposes only. The software polls the status register and if the KNOB INTERRUPT is high in bit 7 of hex address 30A, software reads the status of the 2 input channels in bits 4 and 5 of the same register. Software keeps track of these bits and can determine which one changes first to determine the direction. The software to keep up with the knob rotation and in which direction it is turning.

14.18 BLOCK DIAGRAM

The following diagram is a block diagram of the digital section of the LNA color design.

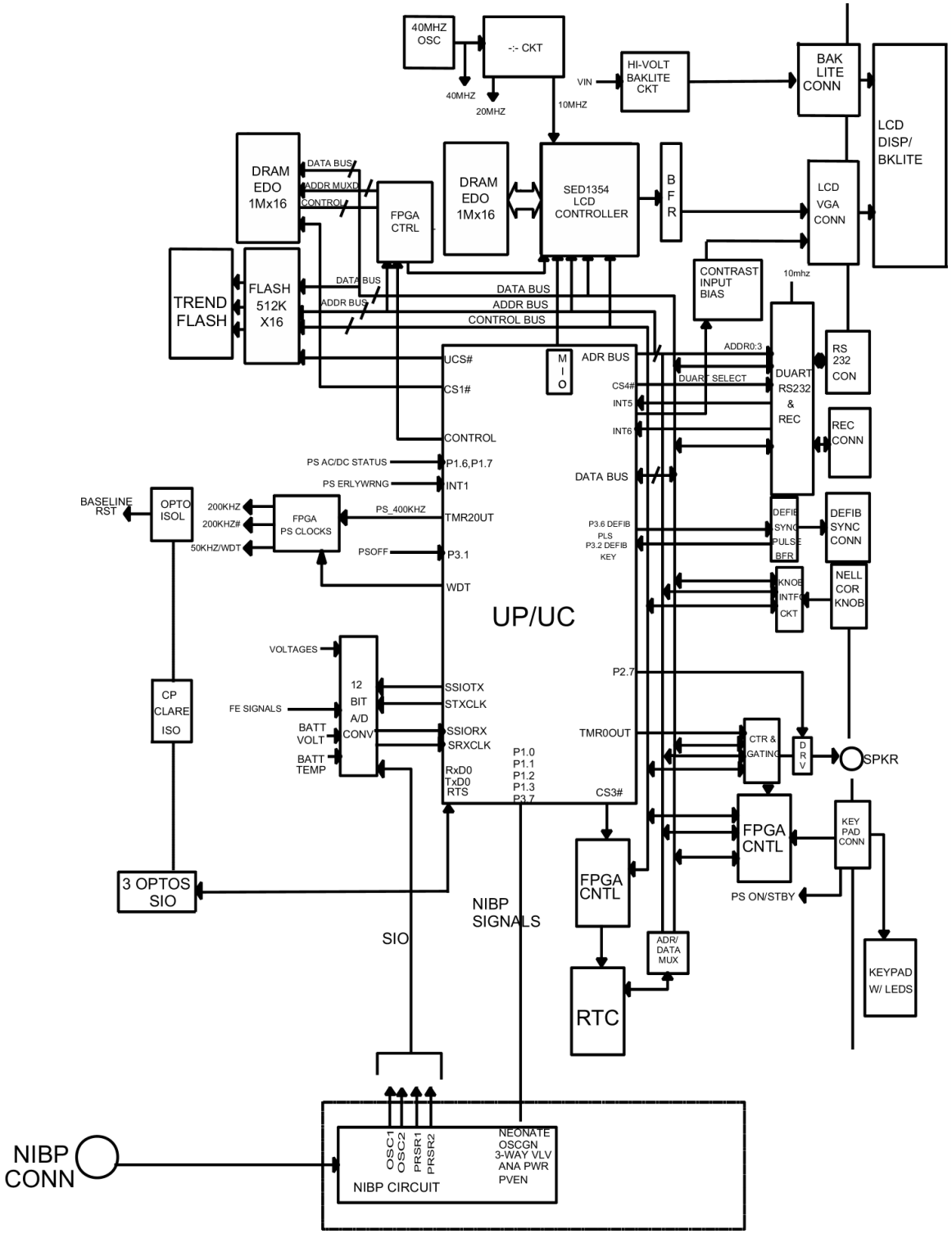

Figure 14-14: NPB-4000C Color Motherboard Block Diagram

14.19 CURRENT DRAIN OF DIGITAL ELECTRONICS

The worst case current drain has been determined by using the maximum numbers in the data sheets of the devices. Typically the devices operate significantly lower.

386EX	130 mA
16M DRAM	170max2=340 mA
8M FLASH	20 mA
LCD CNTLR	30 mA
DUART	3 mA
RS232 XCVR	5 mA
256K FLASH	15 mA
RTC	15 mA
40mhz osc	9 mA
subtotal	567 mA
misc. logic	78 mA
grand total	**645 mA**

power = 3.3 volts x 645 mA = 2.12 Watts worst case

Typical numbers are 3.3 volts at 300 mA = 0.99 Watts.

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SECTION 15: POWER SUPPLY - THEORY OF OPERATION

15.1 Overview
15.2 AC Mains Flyback Power Supply
15.3 Battery Charger
15.4 Buck Converter Operation
15.5 Power Devices
15.6 Miscellaneous Control
15.7 System Power Supply
15.8 Mains (AC) LED Operation
15.9 Power Supply Control Logic
15.10 Alarm Section
15.11 NIBP Pump Control
15.12 Safety Devices

15. POWER SUPPLY - THEORY OF OPERATION

15.1 OVERVIEW

15.1.1 Three Power Supplies

See Figure 15-1 and

Figure 15-2. The NPB-4000/C power supply, as shown in the block diagram, consists of three power supplies and some control logic. The three supplies are:

AC Mains Supply - Accepts universal AC input power (90 - 264 volts RMS, 47-63 Hz). Provides safety line isolation, and produces 18 volts DC at 2 amps (36 Watts) for the Battery Charger.

Battery Charger - Accepts input from either an external DC source (vehicle battery) of 10-16 volts DC, or from the output of the AC Mains Supply (18 volts DC). Provides a tailored charging profile for the NPB-4000/C lead-acid, 3-cell battery. Includes current limiting and temperature compensated float voltage. Maximum output, 7 volts DC at 3.5 amps (24.5 watts).

System Power Supply - Accepts input from the internal NPB-4000/C battery (5.4 to 7 volts DC) and produces regulated outputs of +12, +5, +3.3 and -24 volts DC for NPB-4000/C system usage. Maximum total output power is 25 watts distributed among the four outputs. This peak power occurs only briefly during NIBP pump and printer operation. Typical output power is about 8 watts.

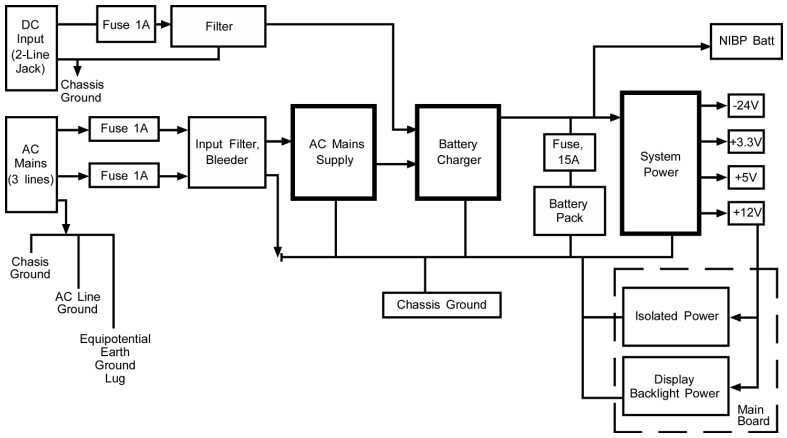

Figure 15-1: Power Supply Block Diagram

Control logic on the power supply assembly is responsible for several system functions:

- AC and DC charging LED drivers
- System ON/OFF control from the front panel membrane switch
- Early Warning OFF notification to the processor board
- OFF on command from the processor board
- Alarm driver based on processor fault (watch dog time-out)
- Alarm Silence from front panel
- NIBP Pump control from logic levels
- Battery Voltage transmittal to the processor board

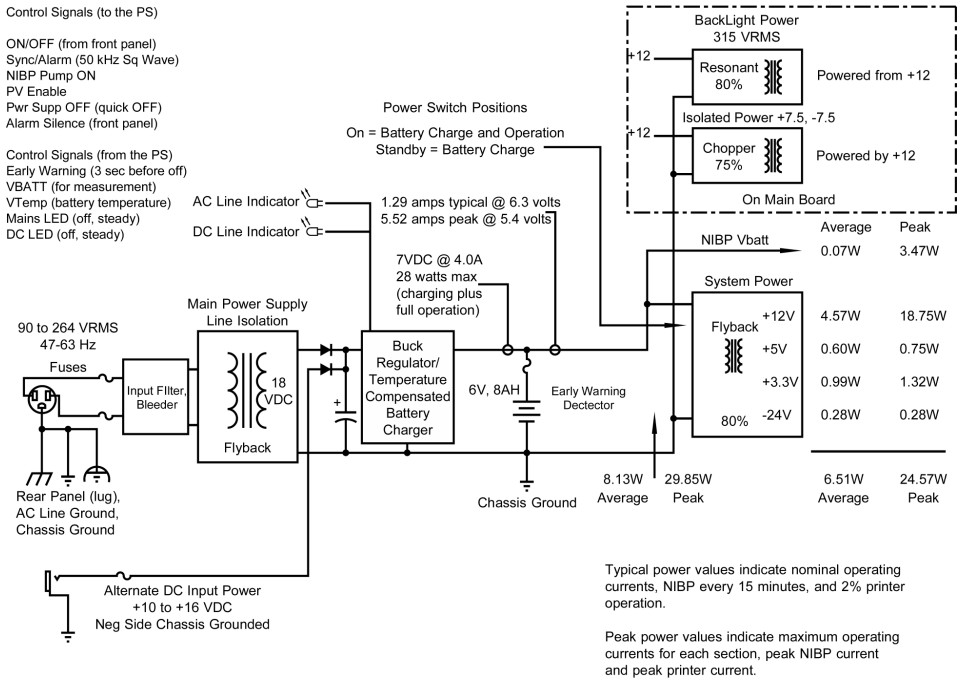

Figure 15-2: Power Supply Detail Diagram

15.2 AC MAINS FLYBACK POWER SUPPLY

15.2.1 Overview

The AC (mains) power supply accepts 90 to 264 volts RMS at 47 to 63 Hz and provides 18 volts DC at a maximum of 2 amps into the battery charger circuit. The 18 volts DC overrides any supplied external DC (10-16 volts DC) and becomes the dominant source to the charger when both external AC and DC are present.

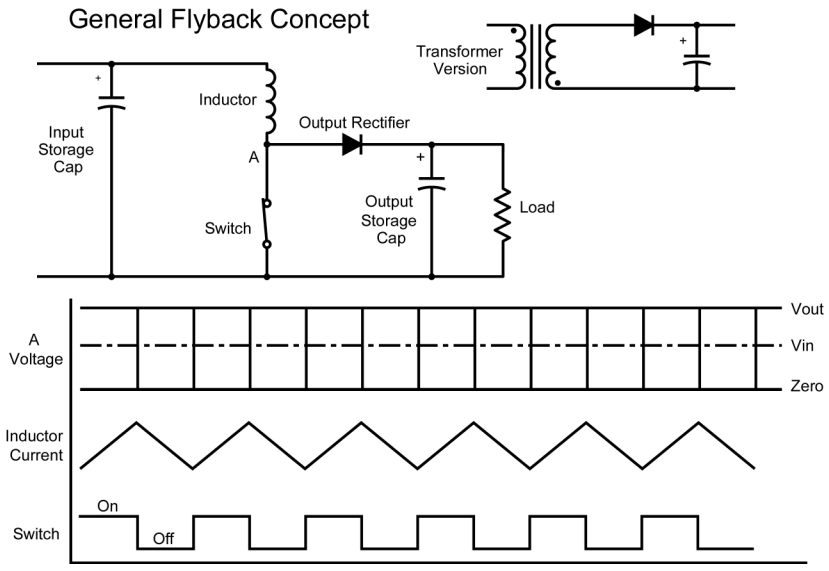

Figure 15-3: General Flyback Circuit Concept

15.2.2 Flyback Principles

See Figure 15-3. In a general flyback circuit, energy is stored in an inductor and transferred to a load during switching cycles. In the first part of the cycle, the switch is closed, the input voltage is applied to the inductor, and current builds linearly. When the switch opens, the voltage at point A (which was grounded) "flies back" up until it hits the output diode. The energy stored in the inductor now depletes into the load.

In the NPB-4000/C power supply, the inductor is a transformer which provides both isolation and a step-down function to reduce the output voltage as required.

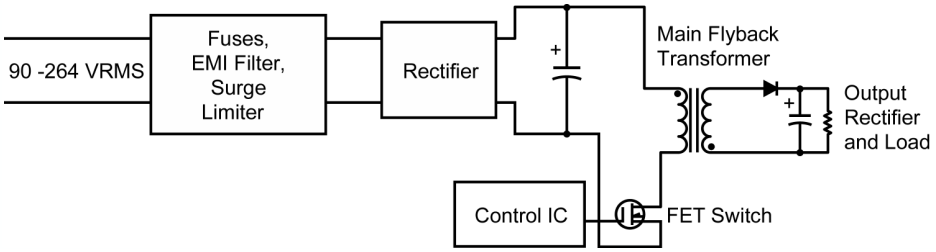

Figure 15-4: AC Power Supply Block Diagram

See Figure 15-4. The NPB-4000/C AC supply runs from a universal AC input and has EMI filtering, rectification, and capacitive storage to provide 100 to 350

volts DC to the flyback circuit. A control IC runs the FET switch, while the transformer (used as an inductor) stores energy and transfers it to the load.

15.2.3 Input filter and Rectifier

The input EMI filter consists of an external "canned" EMI filter assembly (common-mode choke plus X capacitors) that is external to the NPB-4000/C power supply PC board, plus an on- board filter consisting of an L1 common-mode choke with C1 and C2 as X capacitors and C7 and C8 as Y capacitors. Resistor R1 bleeds off any residual voltage on C1 and C2 after the connection to input AC is broken. Surge Limiter R16 limits the initial current through the AC Front End on a cold start when C3 is completely discharged. Fuses F1 and F2 offer safety breaks for both sides of the input line. Diode bridge D1 rectifies the incoming AC to produce a DC voltage from 100 to 350 volts DC at C3.

15.2.4 Controller

The input controller (U1) is a two-loop (current and voltage) controller that forms a fixed frequency variable duty cycle PWM flyback power supply by operating the main switching FET Q1 to regulate the voltage across C12. Controller U1 draws minimal current before operation starts. Initial controller power builds up on C4 from the current supplied by R14 and R15. When U1 begins to operate (at about 10 volts DC), the primary tap (T1, pin 3) supplies power through D4 for the controller. The primary tap also creates the voltage on C12 which is regulated by the controller to 11 volts DC. The transformer secondary is indirectly regulated by turns ratio and magnetic coupling to provide about 18 volts DC.

Resistor R11 and capacitor C14 set the fixed operating frequency (about 100 kHz) of the converter. Current loop feedback enters the controller from current shunt R6, which produces a peak signal of 1 volt with a 1.5 amp primary current. Current limiting (short protection) occurs when the ISNS pin of the controller reaches 1.1 volts. The current waveform is filtered by R8 and C15 to drive the ISENSE input of the controller. Feed-forward resistor R13 provides a bias that lowers the current limit setpoint as the primary input voltage rises. The controller voltage error amplifier works with an internal 2.5 volt reference to regulate the voltage at pin 2 at 2.5 volts. Attenuator R10 and R12 scale the 11 volts DC down to 2.5 volts DC for the error amplifier. Error amplifier compensation is provided by C11, C17, and R9.

15.2.5 Power Devices

The switching FET is driven through R4 (to eliminate the possibility of bipolar latch-up of the output stage). Leakage inductance energy from the transformer primary is caught by D2 and C9, and dissipated in R2. Capacitor C16 and resistor R7 help to damp spurious ringing and lower EMI radiation.

The transformer output is rectified and filtered by D5 and C18. Capacitor C10 and resistor R17 serve to damp output leakage inductance ringing.

15.3 BATTERY CHARGER

15.3.1 Overview

The NPB-4000/C power supply contains a battery charger circuit that accepts DC input from either the isolated AC mains flyback circuit or an externally supplied DC input (10 to 16 volts DC). The output of the battery charger provides a current limited, voltage regulated, temperature compensated output to charge a 6 volt, 8 AH lead-acid battery.

15.4 BUCK CONVERTER OPERATION

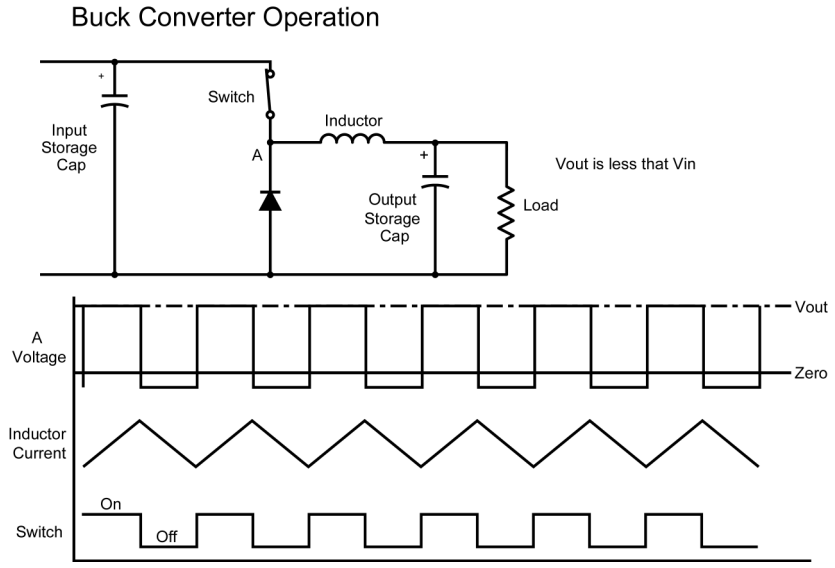

Figure 15-5: Buck Converter Circuit

See Figure 15-5. The battery charger is a buck-switching converter design. In a buck converter (which provides a reduced, or bucked, output voltage) a series switch applies the input voltage to the output through an inductor. When the inductor current has built to a level sufficient to satisfy the load, the switch is opened. The current flowing in the inductor causes the input lead to fly down until it is caught by the catch diode at a voltage slightly below ground. The inductor current then diminishes until the switching cycle is repeated.

The battery charger receives input DC either from the external DC supply (10 to 14 volts) or the AC main supply which provides 18 volts DC. Dual diode D5 essentially acts as an OR gate, allowing the highest voltage to charge C18. Thus the complete input DC range on C18 is from about 10 to 18 volts DC.

15.4.1 Controller

Controller U2 receives its power directly from the input source. Controller U2 will begin operation when the available input voltage is above 9 volts DC. The frequency of PWM operation (about 100 kHz) is set by R26 and C22. Capacitor C69 charges slowly and provides soft start operation by slowly raising the current limit of the controller by clamping the COMP pin through D35.

Switch current information comes from current transformer T2 that provides a current through R29, which is 1/100 of the main switch current. Thus 1 volt across R29 represents 3.4 amps of switch current. The current waveform is fed through an RC filter (R20, C23) to the controller. The controller limits the output current when the ISNS pin reaches about 1.1 volts, or about 3.5 amps average output current.

15.4.2 Float Voltage Regulation

When not in current limit, the controller regulates the VFBK pin to +2.5 volts based on an internal reference. Resistors R25 and R28 attenuate the output voltage to 2.5 volts DC. The thermistor R52 in series with R51 provides voltage setpoint modulation based on the thermistor resistance. The nominal regulated voltage setpoint at 25˚C is 7.05 volts DC. With a 3-cell battery, the nominal charged cell voltage is thus 2.35 volts at 25˚C. The temperature compensation of the battery charger adjusts the output voltage to match (three times) the recommended charged cell voltage as shown in Figure 15-6.

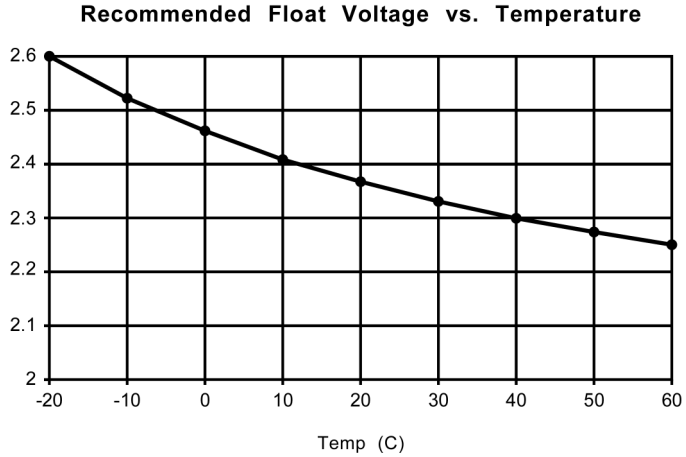

Figure 15-6: Float Voltage vs. Temperature

Capacitor C42, resistor R27, and capacitor C24 provide frequency compensation for the voltage error amplifier.

15.4.3 Drive Translator

The switch control output of the controller does not drive the buck switch directly, but through the inverting driver U3. The series buck switch is P-channel FET Q2. The switch is on when the gate is pulled down toward ground from the DC input rail. Because the gate voltage rating is limited to 15 volts, and the charger input voltage (DCSRC) may exceed 18 volts, we have added a driver voltage regulator consisting of emitter follower Q5 with Zener D9, which keeps the voltage from driver U3 limited to 12 volts under all input voltage conditions. Diode D7 couples the switch control signal from the controller to the driver.

15.5 POWER DEVICES

The switch connects the input source to inductor L3 through current transformer T2 and a section of diode D10. A second section of D10 acts as the "catch" diode in the buck converter. The output voltage is built up across C20 and applied directly to the battery. The series section of diode D10 has been added

to the basic buck-converter diagram to prevent back driving of the circuit from the battery when not charging. Diode D20 acts as a lightweight "catch" diode for the small inductance of the current transformer.

15.6 MISCELLANEOUS CONTROL

The voltage regulation attenuator R28/R25 loads the battery when the circuit is not powered, so voltage sensing of the output voltage occurs using Q6 as a switch to connect attenuator resistor R28 to the output voltage. When the controller is running, it produces a reference voltage (+5 volts) from VREF. This turns on Q3, which pulls 4 ma. from R24, saturating Q6.

A characteristic of buck regulators is an "oscillation" that occurs when the duty cycle exceeds 50 percent because of the flattening of the effective output inductor current slope. The classic method of solving this problem is called "slope compensation" whereby an enhancing slope is summed with the inductor current slope. Slope compensation is applied here by emitter follower Q4 which injects a portion of the oscillator timing ramp into the current loop.

15.7 SYSTEM POWER SUPPLY

The system power supply is a flyback design like the AC mains supply, but it is non-isolated, runs from a DC input of 5.2 to 7.5 volts, and produces multiple output voltages.

The main switching FET (Q8) in the system supply requires +12 volts gate drive for low on resistance (efficient operation), so the controller IC (U4) is powered from the +12 volts DC output generated by the operating supply.

15.7.1 Voltage Doubler

In order to get started, we have a voltage doubler to pump up the battery voltage until supply operation has commenced. When the /PWRUP signal goes low, the startup sequence begins. Transistor Q12 goes on, providing the battery voltage to doubler U5. Doubler U5 is a dual-inverting power driver, and one section acts as an oscillator with negative feedback provided through R44 and C41. The output of the oscillator (/OUTA) is applied to the second inverting driver section resulting in the /OUTB signal. Capacitor C68 provides positive feedback hysteresis to ensure consistent high duty cycle oscillation. When /OUTB is low, C39 is charged to the battery voltage through R42 and D19. When /OUTB is high, the top of C39 is at twice the battery voltage and dumps its charge into C30 through D16. In a brief period, C30 will have built up enough voltage for controller U4 to start, and thereafter U4 receives its power from the +12 volt system output through D16.

15.7.2 Controller

The oscillator in U4 runs at about 40 kHz, set by C37 and R39. When the entire system is running, an external 50 kHz sync pulse is applied to C45, which creates a pulse on R47 to synchronize supply operation to the external signal. Capacitor C34 charges slowly and provides soft start operation by slowly raising the current limit of the controller by clamping the COMP pin through D18.

Controller U4 is a two-loop controller, current and voltage. Input current information is supplied by transformer T4 which with its 100:1 turns ratio produces 1 volt across R31 at 15.4 amps of peak switch current. Current limit is established by U4 at 1.1 volts or 17 amps peak. This peak current equates to about 5 amps maximum average input current.

The voltage loop of U4 regulates the +3.3 volt output through attenuator R41 and R40 which provides 2.5 volts at U4, pin 2. The internal U4 reference and error amplifier regulates this voltage, while C35 and gain limiter R38 provide loop compensation.

15.7.3 Power Devices

Controller U4 drives the switching FET Q8 through R37 (to prevent bipolar latch up of U4). The switching FET builds current in the system transformer, monitored by current transformer T4. When the main FET shuts off, C32 and R36 provide rise-time limitation and leakage inductance snubbing. Leakage current energy is caught by D17 and transferred to C25/C33. Transistor Q7 acts as a switch that turns on when the supply is running to shunt the leakage energy (through R34) to the +12 volts DC supply output. This output (+12 volts) always has a load (from the NPB-4000/C isolated Front End).

The transformer secondary has four rectified outputs to produce +12, +5, +3.3 and -24 volts DC. The -24-volt winding has snubbing (R35, C31) to damp secondary leakage inductance ringing.

15.7.4 Control Circuits

The system supply is turned ON and OFF by the PWRUP/ signal that controls Q11 and Q12. The supply is started when Q12 turns on, powering the voltage doubler to start the controller. When the supply turns OFF, the voltage doubler is stopped, but by that time, the supply is powered from the +12 output. Transistor Q11 now comes into play, dropping the output of the error amplifier (through the COMP pin of U4) to stop system supply operation.

15.8 MAINS (AC) LED OPERATION

The NPB-4000/C monitor has a front panel LED indicator that shows when AC is connected to the unit and charging is underway. The DC input to the charger powers comparator U14. When there is no external DC input (DCIN is low), the comparator output is low. The low output turns on Q29, which powers the MAINS LED indicator from the +5 reference (CVREF) of the charger IC.

15.8.1 External (DC) LED Operation

The NPB-4000/C monitor has a separate front panel LED indicator that shows when external DC is connected to the unit and charging is underway from this source. When external DC is the source for the charger input voltage, the section of D5 that is connected to the external DC is forward biased. Comparator U14 senses that condition and opens its open collector output. Resistor R98 pulls the output up to the +5 volt reference at CVREF and drives the MAINS LED through emitter follower Q23.

Neither LED is driven until CVREF is up, indicating that sufficient power is reaching the charger.

15.9 POWER SUPPLY CONTROL LOGIC

When the battery is initially attached to the power supply, an R/C circuit produces a single positive pulse (PWRRST) which ensures that the power and alarm circuits are initially OFF.

15.9.1 ON/OFF Control

The NPB-4000/C system power supply is turned ON and OFF by alternate pushes of a membrane switch on the front panel. This membrane switch is pulled up to the battery voltage through R61, buffered, and filtered by R62/C52. The conditioned signal toggles flip flop U8 (pin 1) with alternate switch pushes.

The second section of flip flop U8 (pin 12) produces the actual system power supply ON/OFF control signal. The ON signal from U8 (pin 1) produces a brief positive pulse at U8 (pin 8) that turns the system supply ON.

If the push-switch switch is pushed to turn the supply OFF, U12 (pin 1) will go low. While the system supply is running, U12 (pin 2) will also be low. These two low levels cause U12 (pin 3) to be low, which removes the RESET condition from oscillator/divider U10. Oscillator U10 will begin to oscillate and will produce a positive edge on its Q14 output after about 1 second. This edge will clock a low into U8 (pin 11), shutting off the system supply.

15.9.2 Early Warning

The one-second delay between the request for OFF from the push-button and the actual OFF action is called the early warning delay. This delay period allows the processor on the Main Board to store data and make a graceful shutdown before system power is lost. The power supply provides an early warning signal to the Main Board via U11 (pin 6) and Q14 to alert of the pending shutdown.

The processor board can shut down the system power supply on command, without any action from the front panel ON/OFF button. This occurs through the PSOFF line (active low), which produces a high level on U12 (pin 5). The resulting high on U8 (pin 10) directly shuts off system power. In general, the processor has two reasons for shutting power down: either to truncate an early warning cycle, or to halt operation under extreme low battery conditions.

15.9.3 SYNC Pulses

The system power supply runs at about 40 kHz without external synching, but will move up to 50 kHz operation with an external clock signal. The external sync signal from the processor drives Q16, which produces a 5-volt signal on its collector that synchronizes the main supply through C45.

15.10 ALARM SECTION

15.10.1 Alarm Control

When the supply is first turned on, R82 tries to charge C54. During the 300-500 milliseconds charge-up time, it is expected that the supply will come into operation, and the processor board will return sync pulses. The sync pulse will drive Q20 to discharge C54. If the sync pulses stop for any reason, C54 will rise, which will activate the alarm sounder and shut off the supply.

Flip flop U9 latches an alarm condition and is also used to stop a sounding alarm. The flip flop is reset by PWRRST, or by a push of the front panel SILENCE push button.

15.10.2 Alarm Sounder

A SET condition of U9 will turn on FETs Q21 and Q22. With power applied, timing U13 will oscillate and drive the speaker lead with the alarm waveform.

15.11 NIBP PUMP CONTROL

The power supply mechanical assembly holds the blood pressure pump and shield. The power supply contains circuitry that allows logic level control of the pump power from the processor board. For single point fault protection, the pump requires two signals (PUMPON and PVENB) to activate the pump. The PUMPON signal (when high) turns on the N-channel FET section of U15, which pulls the bottom lead of the motor to ground. The PVENB signal, through level translator Q19, turns on the P channel section of U15, which pulls the top motor lead to VBATT.

Diode D32, capacitor C46, and resistor R77 provide noise control during motor operation.

15.12 SAFETY DEVICES

A number of safety devices serve to limit the severity of fault-induced problems.

- Fuse-Limited AC high input lead
- Fuse-Limited AC Low input lead
- Fuse-Limited external DC input lead
- Fuse-Limited VBATT lead for system supply operation
- Polyswitch® (self-resetting fuse) protected VBATSNS lead for control logic and Main Board usage
- Two signals and two paths required to activate the NIBP pump
- Short-circuit protected AC Mains Supply
- Short-circuit protected charger
- Short-circuit protected system supply (current-limiting and three polyswitches)
- Alarm sound if processor fails

15.12.1 Watchdog Shutoff

Another shutdown path exists for the system supply. When the system supply begins operation, PWRUP goes high, which begins to charge C49 through R65. Eventually (0.5 second), C49 will charge up (through U12) and the system supply will shut off.

The way that the supply is kept running is through the receipt of a SYNC/ALARM pulse from the processor board. This 50 kHz square wave from the processor has two purposes: it synchronizes the switching frequency of the system power supply, and its absence indicates a time-out of the watch dog timer in the processor section. Transistor Q16 produces a 5-volt pulse for synching the supply, and the periodic pulsing allows Q15 to keep C49 discharged. If the sync pulse disappears, the system supply will keep running for a while (based on its own R/C oscillator), but the rising voltage on C49 will shut the unit down in a few hundred milliseconds.

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SECTION 16: MP-205 SERVICE MANUAL (NPB P/N: 044540A-0296)

16.1 Overview
16.2 Module Description
16.3 Circuit Description
16.4 Interconnections
16.5 Sensor Interconnect
16.6 *Oxichip* Circuit
16.7 Preamp
16.8 Programmable Gain Amplifier (PGA), Demodulator and Demultiplexer
16.9 Filters and Level Shifter
16.10 LED Driver
16.11 Reset Schmitt Trigger
16.12 High Resolution A/D Converter
16.13 Input Filter
16.14 Power Decoupling
16.15 Status and Timing
16.16 Analog Power Regulation
16.17 Microcontroller
16.18 Troubleshooting The MP-205
16.19 Packing for Shipment
16.20 JMP-205 Specifications

16. MP-205 SERVICE MANUAL

16.1 OVERVIEW

This section contains technical and service information for the Nellcor pulse oximetry module, model MP-205. This product is to be serviced only by qualified service personnel.

16.2 MODULE DESCRIPTON

The MP-205 is a printed circuit module containing signal processing circuits to measure oxygen saturation and pulse rate based on signals supplied by Nellcor oxygen transducers (sensors) connected to the host system and applied to a patient.

The MP-205 is built around an 80C552 microcontroller, and has been implemented using low-power design techniques. The module consumes approximately 0.5 Watts.

The MP-205 incorporates *C-Lock*® ECG synchronization to allow measurements on patients with low perfusion, or in the presence of patient motion. An ECG synchronization signal can be brought into the module via a hardwired connection or a real-time software input. ECG synchronization processing can be enabled or disabled by software.

The host system supplies analog outputs, parallel input/output, LCD display drive, patient-isolated power, and alarms.

16.3 CIRCUIT DESCRIPTION

This section provides service personnel with an explanation of the circuit operation for the oximetry module. The text is supported with a schematic diagram, see Figure 17-1.

16.4 Interconnections

16.4.1 Host (Monitor) Interconnect

The monitor interface is a 14-pin dual-row header connector, JP5. This connector includes the power supplied by the host monitor, a serial interface port, and two hardware control lines. The power required by the oximetry module is +5 volts (digital) and ±5 volts (analog).

Other than supply voltages provided to the module from the power supply, there are five data signals present at the module connection to the monitor, see Figure 17-1.

CTS*	clear to send is a logic signal (active low) transmitted to the module by the monitor to suspend data transmission from the module.
EXT_RESET*	an asynchronous input (active low) from the monitor to effect a reset in the oximetry module; CR3 provides a voltage protection from the power-on reset.
RXD	the receive data line to the oximetry module.
TXD	the transmitted data line from the oximetry module; U6 provides a buffer for this signal.
C_LOCK	a hardwired timing pulse (active high) transmitted to the oximetry module, via the host instrument, from an external ECG monitor. The rising edge of this pulse is used by the module to satisfy the software requirements necessary to perform pulse recognition using ECG as a timing reference.

NOTE: " ***** " indicates a LOW active signal.

16.5 Sensor Interconnect

The sensor interface is a 10-pin dual-row connector, JP1, located on the oximetry module PCB.

16.6 *Oxichip* Circuit

At the heart of the oximetry module is the U1 *Oxichip*™ integrated circuit, which provides variable LED drive, photodetector amplification, variable gain, demodulation, filtering, and signal conditioning for the analog-to-digital converter (ADC) input. The *Oxichip* circuit generates its own LED modulation and photodetector demodulation timing. It requires only a single clock at 8-times the desired LED switching frequency. A block diagram of the *Oxichip* circuit is shown on Figure 17-2.

In the following discussion, parts that are internal to the *Oxichip* circuit are noted with a "U1." prefix.

16.7 Preamp

The current-to-voltage (I-to-V) converter has a gain of -249 K V/A and a low-pass corner frequency of 30 kHz. The voltage amplifier has a gain of -2 V/V and a low-pass corner frequency of 20 kHz. The voltage amplifier is disconnected from the I-to-V converter during LED switching transients to prevent transmission of the switching spikes into the programmable gain amplifier (PGA).

The ambient light canceller (ALC), which consists of U1A3, R6, and C6, generates a current opposing the DC current coming from the photodetector, which is caused by ambient light. The ALC switches on during the Red cycle and has a closed-loop frequency response of 240 Hz. It can cancel up to 36 microamps of DC photocurrent. The response time to a change in LED drive is less than 2 milliseconds.

The RC filter that removes sensor cable noise is comprised of R1 and C49. Component CR4 serves as an ESD-protection diode.

16.8 Programmable Gain Amplifier (PGA), Demodulator and Demultiplexer

The PGA U1A4 provides a variable gain to accommodate a wide range of signal strengths. As the PGA amplifies the signal from the preamp by a programmable gain, the demodulator shifts the frequency down to baseband, while the demultiplexer separates the IR and Red components of the signal. The PGA has a programmable gain from 1 to 128 in powers of 2.

The PGA output goes to the peak detectors for status monitoring and to the demodulator/demultiplexer (U1A5, which is internal to the *Oxichip* circuit) for signal processing.

There are two peak detectors: one detects positive peaks (above the 2.2-volts reference) and one detects negative peaks, or valleys (below the 2.2-volts reference). This measurement point is referred to as COMPARE2, or C2. The peak and valley detector circuitry consists of CR3, R26, R41, R42, R43, C42, and C41.

The response of the peak detectors is nonlinear since the diode CR2 impedance changes as the voltage on the diode changes. The charging time constant is limited to no faster than 20.8 microseconds. The decay time constant is 19.8 milliseconds.

16.9 Filters and Level Shifter

The filters and level shifter circuitry are shown in Figure 17-2.

The 10 Hz filters eliminate the high frequency components of the optical signal and get it ready for conversion to a digital signal, thereby smoothing out the Red and IR signal from the demultiplexer. The gain of the Red filter circuit is eight, while the gain of the IR filter circuit is five.

The Red filter circuit components consist of U1A6-8, R19–21, R31, R34–37, C22, C29–30, and C37–38. The IR filter circuit components consist of U1A10-12, R22–24, R32–33, R38–40, C23–24, C31–32, and C39. The IR filter is identical to the Red filter except for the component values in the last stage.

The level shifter moves the reference for the signal back to ground. The level shifter (U1A9) selects the desired signal and shifts the signal reference from 2.2 volts reference to ground, or 0 volts. This circuit has a gain of two and an intentional offset of 80–120 millivolts at the output.

16.10 LED Driver

The LED driver circuit generates regulated and programmable currents for driving the sensor LED's. The circuit switches the currents in the proper phases of the LED strobe cycle. The IR and Red currents can be programmed independently. The LED currents are generated by forcing a programmable-voltage across R9, then switching the resulting current through the LED's.

The LED driver is almost entirely contained within the *Oxichip* U1 circuit. This driver also has an over-current detection feature that shuts down all LED drive if the average current exceeds 44 milliamps. The over-current trip level is set by passing the LED current through R10 and C9 and comparing the voltage drop to V_{DD}-0.3 volts. Components CR5 and CR6 serve as ESD-protection diodes. See Figure 17-2.

16.10.1 References

There are three voltage references on the *Oxichip* U1 circuit. The 3.125 volt reference is used for Rcal stimulus and the high resolution A/D converter reference. It is a low-impedance output. The 2.2 volt buffered reference is used as the signal ground for the photodetector cathode and is a low-impedance output. The 2.2 volt reference is used for signal ground in the rest of the circuit. It is a high-impedance output and is filtered by C3.

16.11 Reset Schmitt Trigger

The power-on reset function is accomplished with a Schmitt Trigger inside the *Oxichip* U1 circuit and external components R45 and C44. The Schmitt Trigger supplies an active high reset to the processor on RST. Diode CR2 protects the *Oxichip* circuit from the discharge of C44.

16.12 High Resolution A/D Converter

The oximetry module uses a crystal semiconductor CS5102A 16-bit A/D converter for the conversion of the filtered optical signals and for RCAL measurement. This A/D converter is shown in Figure 17-2 as U2.

16.13 Input Filter

The input filter to U2 is through the level shifter circuit, which consists of R18 and C13. The Rcal filter circuit consists of R17, C20 and C21.

16.14 Power Decoupling

The power supply decoupling circuit consists of R29, R30, C16 through C18, C28, and C26 and C27.

16.15 Status and Timing

The LED drive, ALC, demodulator, and demultiplexer require timing signals to operate properly. All of the proper timing sequences are provided by the state machine, the OXICLK signal, within the *Oxichip* U1 circuit. The state machine requires a clock from the CPU at 8 times the desired LED strobe frequency.

16.16 Analog Power Regulation

The oximetry module analog functions are powered by ±5 volts DC. Analog filtering is provided by R15 and R16, and C11 and C12.

16.17 Microcontroller

The oximetry module microcontroller is an 80C552 IC, U4, with 64K ROM, U3, 32K RAM, U7, and an address latch U6. The connection to the *Oxichip* circuit gain settings is through the data bus and the control lines CS* and LE.

Table 16-1: Oxichip Circuit Pin Descriptions

Pin Name	Pin #, type	Signal Description
CS*	1, DI	Chip Select, latches the data bus into the storage registers. Connected to WR* U4P3-6
LE	2, DI	Latch Enable, enables writing to the storage register. Connected to U4.P1-1
CYCLE	3, DO	Indicates whether the *Oxichip* circuit is in a Red or IR cycle. High is Red, low is IR Connected to U4P3-3
CLH	4, LP	High side current limit protection Connects to LED supply voltage through resistor R10 in parallel with capacitor C9.
LEDPOS	5, LO	+LED connection to sensor
LEDNEG	6, LO	-LED connection to sensor
CLL	7, LP	Low side current control. Connects to LED supply return through 10 Watt resistor R9.
GATE	8, DO	Combined gate signal, rising edge initiates a COMPARE A/D conversion. Connects to U4-STADC
SATIN*	9, DO	LED on or off status indicator: high is off, low is on. Connects to U3P4-3.
RESET*	10, DI	Input of Schmitt Trigger for generating a reset.
RST	11, DO	Output of Schmitt Trigger, active high reset pulse.
VSS	12, DP	Digital power return.

Table 16-1: Oxichip Circuit Pin Descriptions

Pin Name	Pin #, type	Signal Description
VSSA	13, AP	Analog power return.
FR3OUT	14, AO	Red filter chain, operational amplifier 3 output.
FR3NEG	15, AI	Red filter chain, operational amplifier 3 inverting input.
FR2OUT	16, AO	Red filter chain, operational amplifier 2 output.
FR2NEG	17, AI	Red filter chain, operational amplifier 2 inverting input.
FR1OUT	18, AO	Red filter chain, operational amplifier 1 output.
FR1NEG	19, AI	Red filter chain, operational amplifier 1 inverting input.
RED	20, AO	Red demodulator/demultiplexer output.
PGAOUT	21, AO	Programmable gain amplifier output.
SOUT	22, AO	Ambient light auto-null amp output.
SINNEG	23, AI	Ambient light auto-null amplifier inverting input.
SWITCH	24, AO	Ambient light auto-null switch output.
A2OUT	25, AO	Photodetector amplifier 2 output.
A2INNEG	26, AI	Photodetector amplifier 2 inverting input.
A1INPOS	27, AI	Photodetector amplifiers 1 and 2 non-inverting inputs.
A1INNEG	28, AI	Photodetector amplifier 1 inverting input.
A1OUT	29, AO	Photodetector amplifier 1 output.
VREF 3125	30, AO	3.125 volt reference output.
31, AO	VREF25	2.5 volt buffered reference output.
32, AO	VREF22	2.2 volt reference output.
33, AO	IR	IR demodulator/demultiplexer output.
34, AI	FI1NEG	IR filter chain, operational amplifier 1 inverting input.
35, AO	FI1OUT	IR filter chain, operational amplifier 1 output.
36, AI	FI2NEG	IR filter chain, operational amplifier 2 inverting input.
37, AO	FI2OUT	IR filter chain, operational amplifier 2 output.
38, AI	FI3NEG	IR filter chain, operational amplifier 3 inverting input.
39, AO	FI3OUT	IR filter chain, operational amplifier 3 output.
40, AO	LS	Level shifted and multiplexed output to ADC.
41, AP	VDDA	Analog power.
42, DP	VDD	Digital power.
43, DI	RED-IR*	Multiplexer select input, high is Red, low is IR, to U4P1-2.
44, DI	CLK_16	Clock speed select, high is 128xfMOD, low is 8xfMOD
45, DI	CLK	Clock input
46, DI	D4	Data bit 4, to AD4
47, DI	D3	Data bit 3, to AD3
48, DI	D2	Data bit 2, to AD2

Table 16-1: Oxichip Circuit Pin Descriptions

Pin Name	Pin #, type	Signal Description
49, DI	D1	Data bit 1, to AD1
50, DI	D0	Data bit 0, to AD0
51, DO	LIM	Overcurrent limit indicator, high indicates current limit has tripped, to U4P4-6.
52, DI	EN*	LED enable, high disables LED drive, low enables LED drive, to U4P1-0.

16.18 TROUBLESHOOTING THE MP-205

16.18.1 Introduction

The MP-205 is a subsystem intended for use with a host system. This section assumes that the host provides a means of communicating with the module through the serial host data interface described in the "OEM Pulse Oximetry Module, Model MP-205, Engineering Product Specification."

16.18.2 Fault Evaluation

Proceed as follows to evaluate and determine possible fault or error sources:

Table 16-2: Fault Evaluation

Indication	Action
No communication	Check cables and interconnections. Check 5-volt digital power supply. Check processor clock Y1. Check TXD buffer U5. Check BAUD rate jumpers.
Error X00 no sensor	Sensor may be disconnected or damaged. Cable between sensor and MP-205 may be disconnected or not functioning properly.
Error P00 pulse search	The sensor may be improperly applied to the patient or may be damaged. Try another sensor. Try an SRC-2 pulse oximeter tester to check MP-205 functionality. Cover the sensor to eliminate the possibility of ambient light interference. The patient's perfusion may be too poor for the instrument to detect an acceptable pulse. Try using *C-lock* ECG synchronization, if available. Check + and –5 volt analog power supplies. Check for proper LED drive function. Check the signal path from the photodetector input to the A:D converter.
Waveform output incorrect	Sensor or interconnecting cables may be damaged. Interrogate module with W00 and determine if the update rate is appropriate. Noise may be present.

The following table lists reported error numbers, the error description, and recommended user action.

Table 16-3: Reported Errors

Error #	Error Description	Recommended Action
E011	RAM error occurred (MP-205 stops normal operation)	Host should not continue operation with the MP-205.
E012	ROM error occurred (MP-205 stops normal operation)	Host should not continue operation with the MP-205.
E013	Last message sent by host had a checksum error (last message or command was discarded)	Serial line may be defective. Check for possible noise on the serial line interface. Verify correctness of checksum calculation. Resend last message to the MP-205. If error persists, MP-205 may be defective.
E014	Write not permitted or command not allowed (command discarded, normal operation continues)	Check command description for valid values. Resend command with correct value.
E015	Module received a command with a value out of range (command discarded, normal operation continues)	Check command description for valid values. Resend command with correct value.
E016	Calibration failed (MP-205 continues with normal operation)	Nonfatal error; host design decides what action to take.
E017	Calibration already in progress (MP-205 continues with normal operation)	Continue processing.
E018	Calibration request denied (MP-205 continues with normal operation)	Continue processing.
E019	Communication syntax error on command sent by host (command discarded; normal operation continues)	Check command description for correct syntax. Resend command with correct value.
E0210	Excessive sensor current was detected (MP-205 stops normal operation and continuously sends this error message)	Notify user to check and/or replace the sensor or cable. Reset or cycle power to the MP-205. Retry saturation measurement with patient. Check for excessive noise on +5 volt digital supply. If error persists, MP-205 may not be functioning properly.

16.18.3 Waveforms

Figure 16-1 through Figure 16-5 are typical waveforms as measured at various test points (labeled TP) on the oximetry module. These waveforms are valuable in tracing signals and locating faults. The user must use a *Nellcor* SRC-2 pulse oximeter tester. Contact Mallinckrodt Technical Services Department if you have difficulty replicating these waveform examples.

16.18.4 SRC-2 Settings

Rate:	112
Light:	High2
Modulation:	LOW
Remote/Local:	RCAL 63

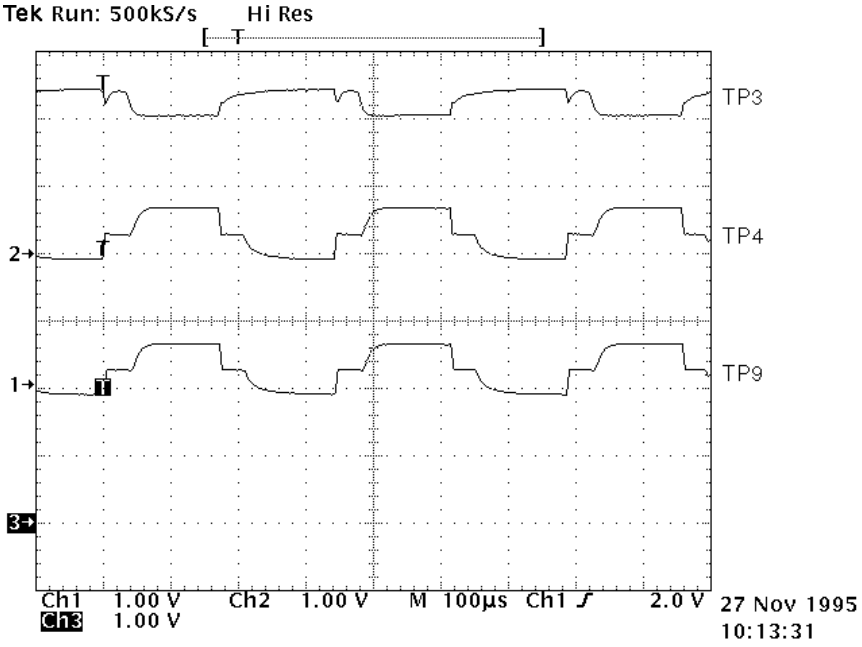

Figure 16-1: Preamplifier and PGA Outputs

16.18.5 Trace Descriptions

CHNL 2 : TP3 Primary Input Preamplifier
CHNL 1 : TP4 Secondary Input Preamplifier
CHNL 3 : TP9 PGA output

16.18.6 SRC-2 Settings

Rate: 112
Light: High2
Modulation: HIGH
Remote/Local: RCAL 63

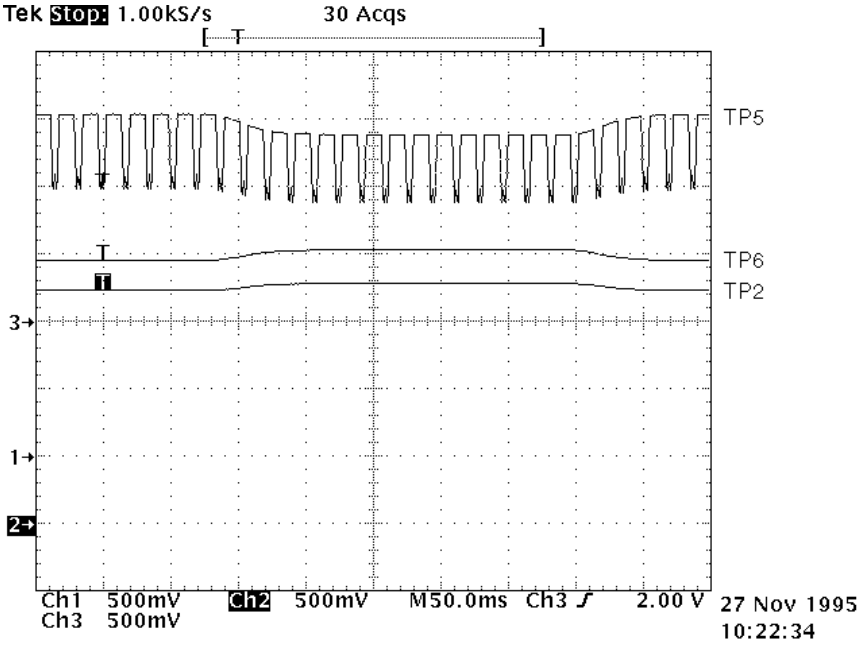

Figure 16-2: Filter Outputs and ADC Input

16.18.7 Trace Descriptions

CHNL 3 : TP5 ADC Input
CHNL 1 : TP6 Red Filter Output
CHNL 2 : TP2 IR Filter Output

16.18.8 SRC-2 Settings

Rate: 112
Light: High2
Modulation: HIGH
Remote/Local: DC RCAL 63

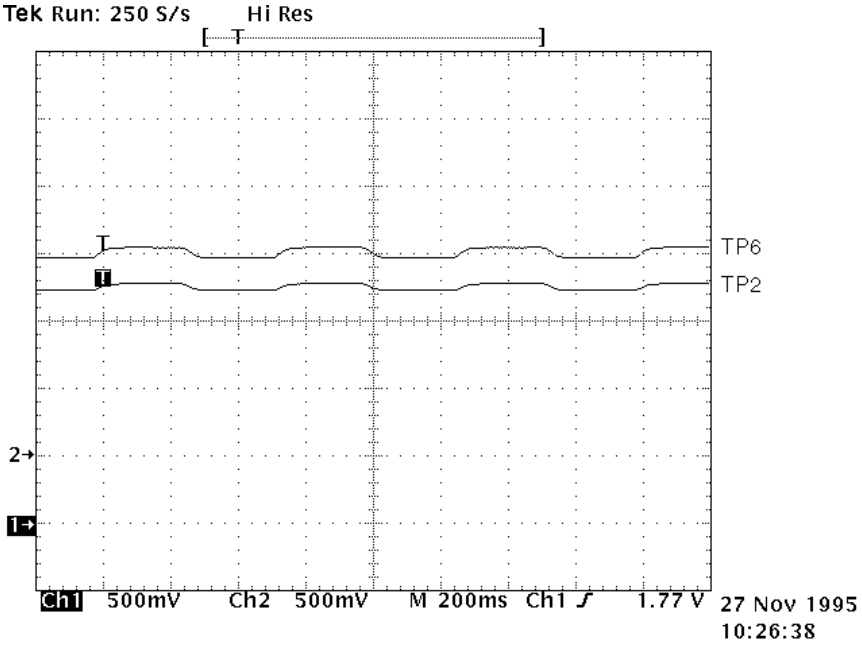

Figure 16-3: MP-205 with an SRC-2 Filter Output

16.18.9 Trace Descriptions

CHNL 2 : TP6 Red Filter Output
CHNL 1 : TP2 IR Filter Output

16.18.10 SRC-2 Settings

Rate: 112
Light: High2
Modulation: HIGH
Remote/Local: DC RCAL 63

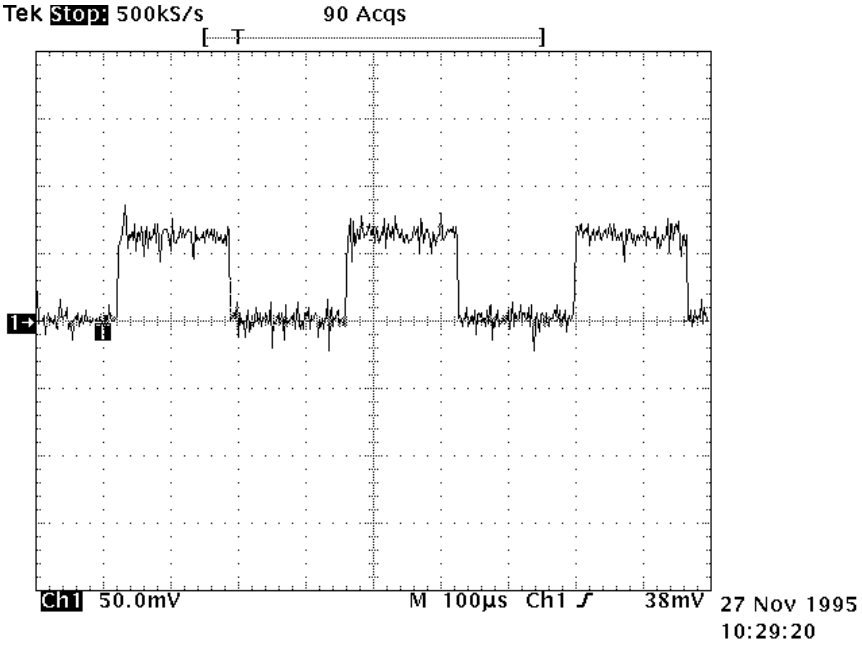

Figure 16-4: MP-205 with an SRC-2 LED Drive Current Test at TP7

16.18.11 SRC-2 Settings

Rate: 112
Light: High2
Modulation: HIGH
Remote/Local: DC RCAL 63

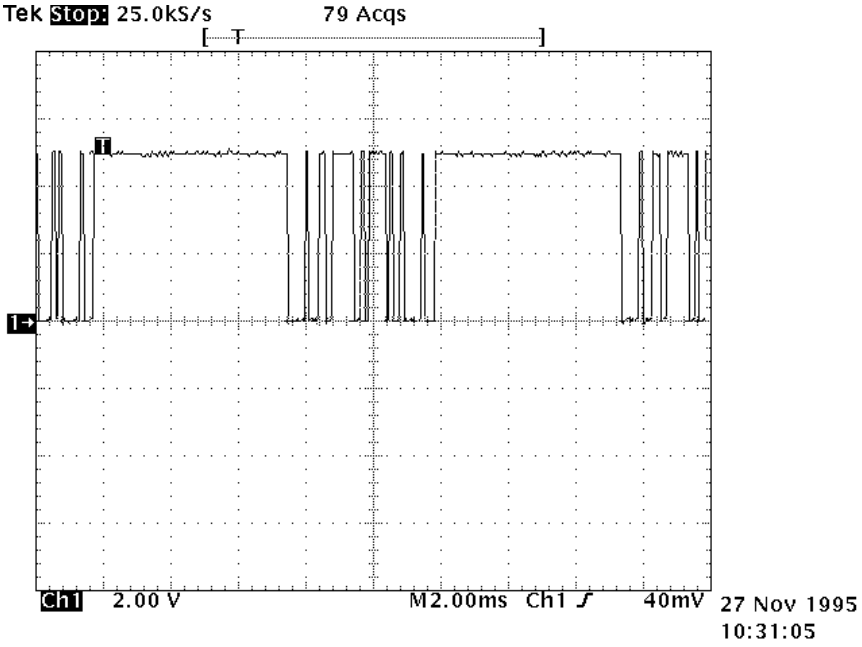

Figure 16-5: MP-205 with SRC-2 Serial Port TXD Signal, U4 Pin 25

16.19 PACKING FOR SHIPMENT

Should you need to ship the oximetry module for any reason, follow the instructions in this section.

16.19.1 General Instructions

Pack the module carefully. If the original shipping carton is not available, use another suitable carton or call Mallinckrodt Technical Services Department to obtain a shipping carton.

Prior to shipping the device, contact your supplier or your local office Mallinckrodt Technical Services Department for a returned goods authorization (RGA) number. Mark the shipping carton and any shipping forms with the RGA number.

16.19.2 Repackaging in Original Carton

If available, use the original carton and packing materials. Pack the module as follows:

1. Place module in original packaging.
2. Place packaging in shipping carton and seal carton with packaging tape.
3. Label carton with shipping address, return address, and RGA number.

16.19.3 Repackaging in a Different Carton

If the original carton is not available:

1. Place module in antistatic bag.
2. Locate suitable corrugated cardboard shipping carton.
3. Fill bottom of carton with packing material.
4. Place bagged unit on layer of packing material and fill box completely with packing material.
5. Seal carton with packing tape.
6. Label carton with shipping address, return address, and RGA number.

16.20 MP205 SPECIFICATIONS

16.20.1 Measurement Range/Accuracy

Range		
Saturation:	1 - 100%	
Pulse Rate:	20 - 250 beats per minute (bpm)	
Accuracy		
SpO_2 [1]		
Adults:	70 - 100%	±2 digits
	0 - 69%	unspecified
Neonates:	70 - 100%	±3 digits
Pulse Rate	20 - 250 bpm	±3 bpm

[1] Accuracies are expressed as ± "X" digits (saturation % points) between saturations of 70 and 100 percent. This variation equals ± one standard deviation (1SD), which encompasses 68 percent of the population. All accuracy specifications are based on testing the subject monitor on healthy adult volunteers in induced hypoxia studies across the specified range. Adult accuracy is determined with *Oxisensor® II* D-25 sensors. Neonatal accuracy is determined with *Oxisensor II* N-25 sensors. In addition, the neonatal accuracy specification is adjusted to take into account the theoretical effect of fetal hemoglobin in neonatal blood on oximetry measurements.

16.20.2 Measurement Conditions

SpO_2 and pulse rate accuracy specifications apply under the following conditions:

- Electrosurgical apparatus not used
- Patient free of injected intravascular dyes
- Insignificant concentration of carboxyhemoglobin and methemoglobin
- Sensor at a temperature between 28º C and 42ºC
- External illumination less than 5,000 lumens/square meter (typical office lighting)
- Response mode set at Mode 1

16.20.3 Sensors

16.20.3.1 Measurement Wavelengths

Red:	660 nm, nominal
Infrared:	920 nm, nominal

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SECTION 17: DRAWINGS

17.1 Overview
17.2 List of Figures

17. DRAWINGS

17.1 OVERVIEW

This section contains circuit schematics for the NPB-4000/C patient monitor.

17.2 LIST OF FIGURES

Figure No.	Title	Page
Figure 17-1	MP-205 PCB Schematic (Sheet 1 of 2)	17-3
Figure 17-2	MP-205 Schematic PCB (Sheet 2 of 2)	17-5
Figure 17-3	NPB-4000/C Power Supply PCB (Sheet 1 of 2)	17-7
Figure 17-4	NPB-4000/C Power Supply PCB (Sheet 2 of 2)	17-9
Figure 17-5	NPB-4000/C Main PCB Schematic (Sheet 1 of 3)	17-11
Figure 17-6	NPB-4000/C Main PCB Schematic (Sheet 2 of 3)	17-13
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Figure 17-8	NPB-4000/C Interconnect Diagram	17-17
Figure 17-9	NPB-4000C Color Motherboard Schematic	17-19

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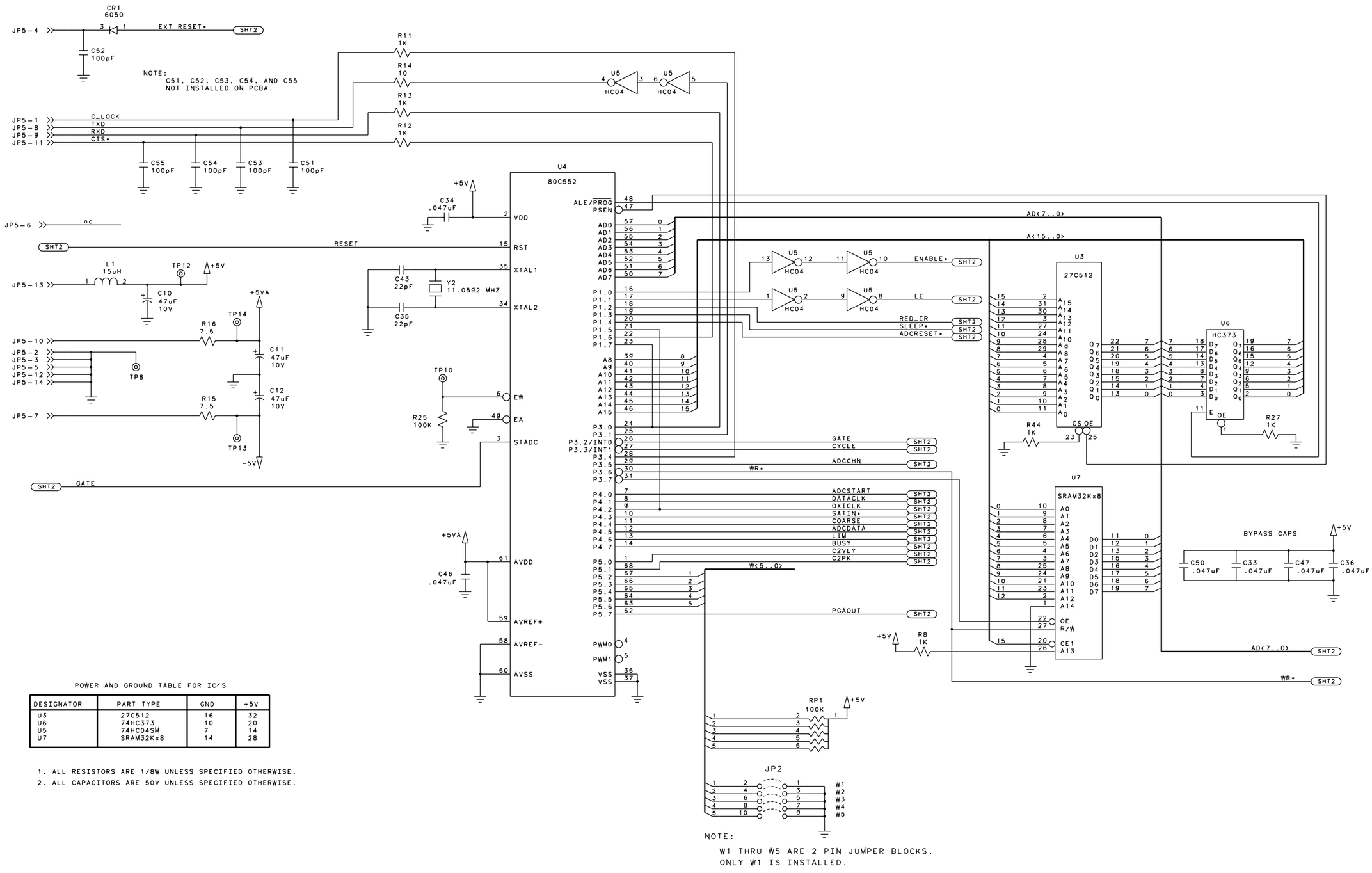

POWER AND GROUND TABLE FOR IC'S

DESIGNATOR	PART TYPE	GND	+5V
U3	27C512	16	32
U6	74HC373	10	20
U5	74HC04SM	7	14
U7	SRAM32Kx8	14	28

1. ALL RESISTORS ARE 1/8W UNLESS SPECIFIED OTHERWISE.
2. ALL CAPACITORS ARE 50V UNLESS SPECIFIED OTHERWISE.

Figure 17-1
MP-205 PCB Schematic (Sheet 1 of 2)

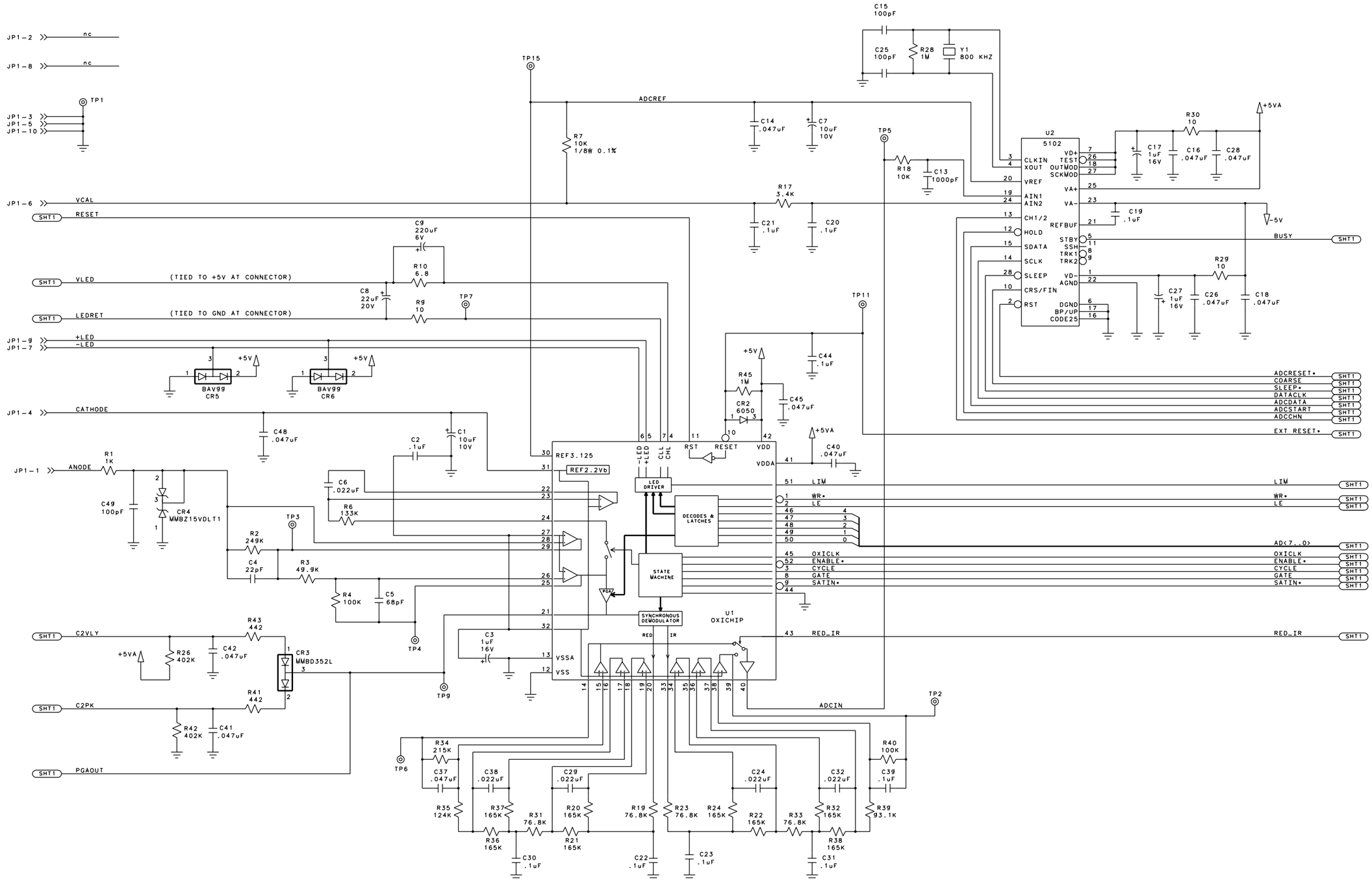

Figure 17-2
MP-205 PCB Schematic (Sheet 2 of 2)

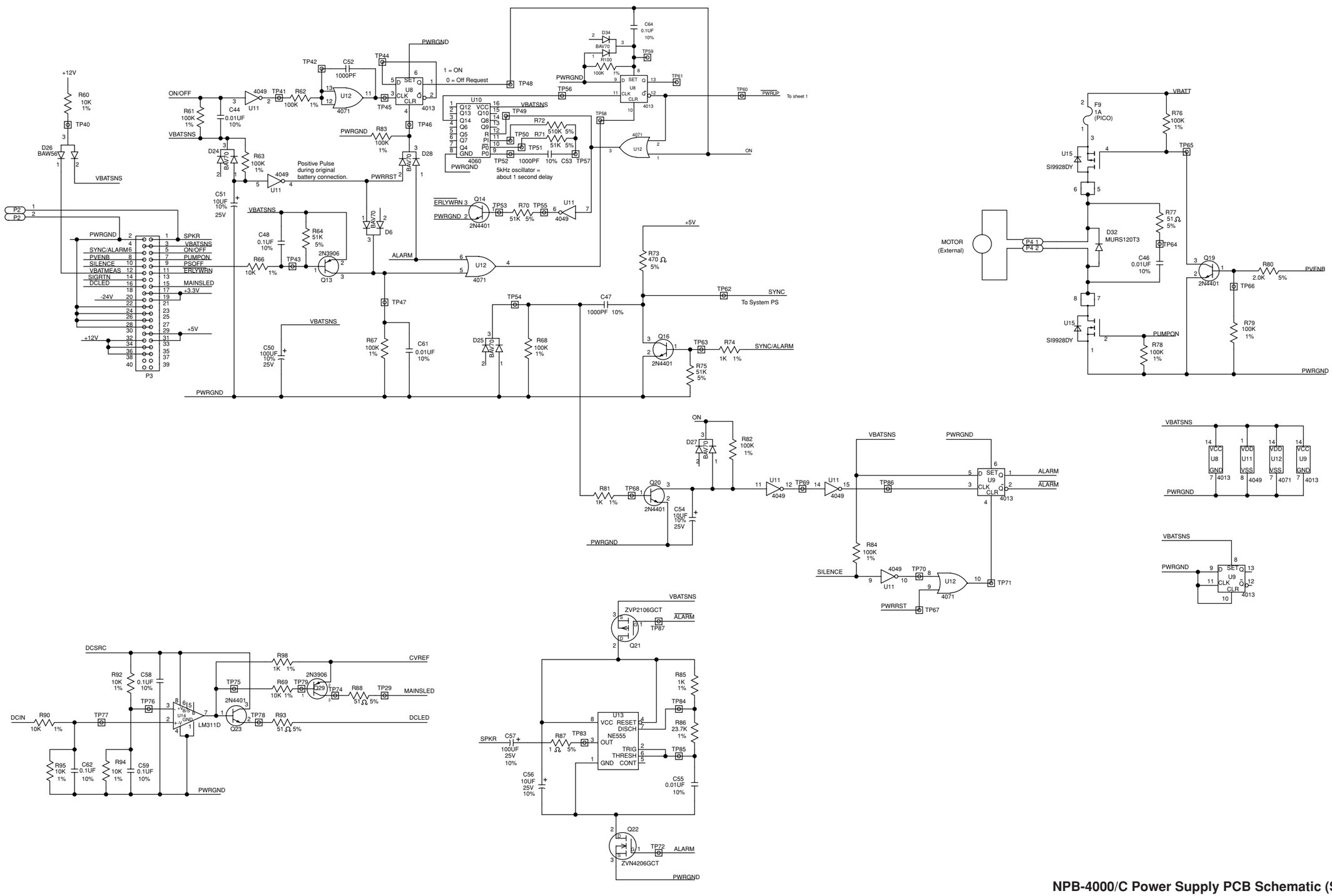

Figure 17-3
NPB-4000/C Power Supply PCB Schematic (Sheet 1 of 2)

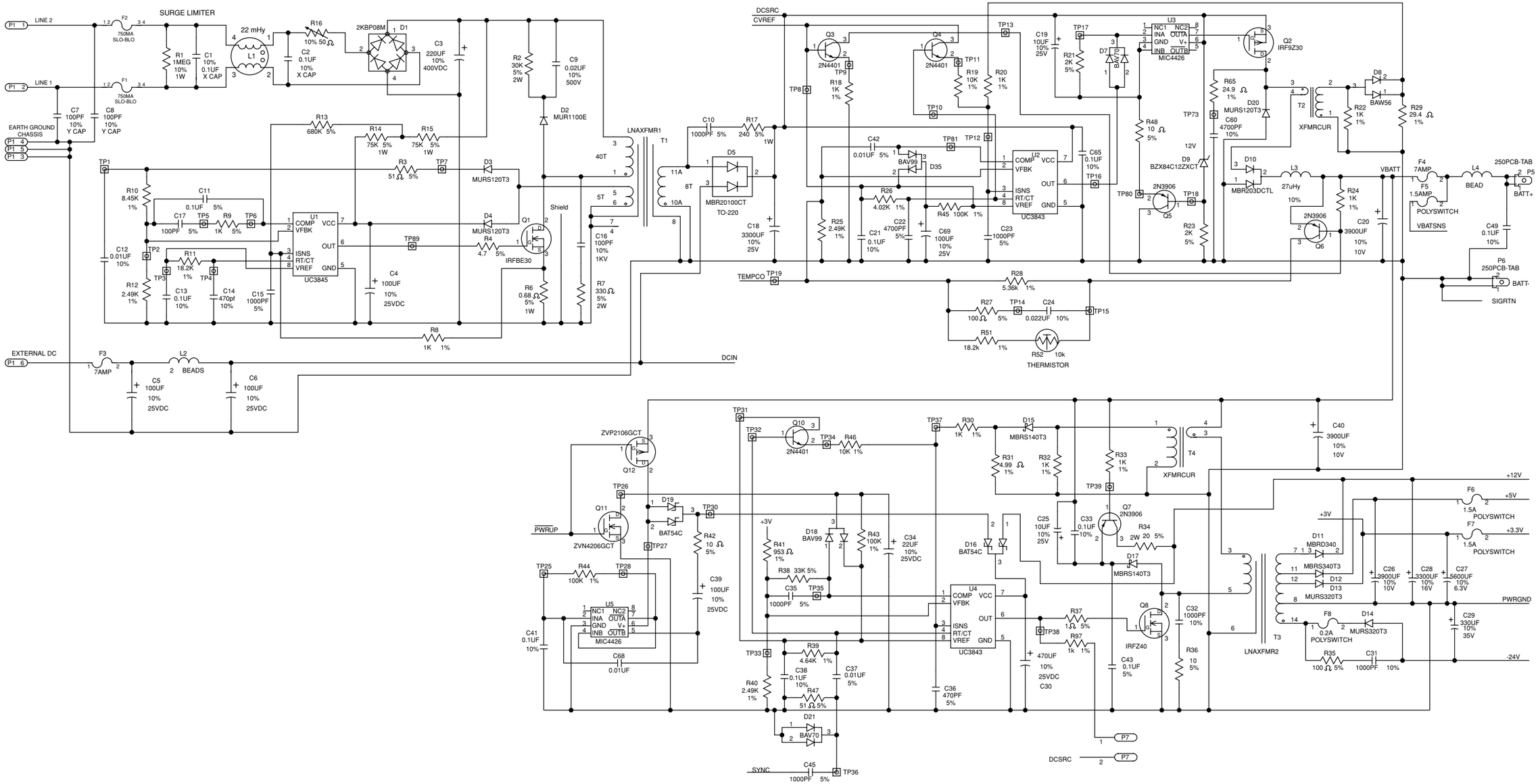

Figure 17-4
NPB-4000/C Power Supply PCB Schematic (Sheet 2 of 2)

J1-LCD CONN.
J2-KEYPAD
J3-50 PIN CONN.
J4-BACKLITE
J5-TEST PTS.
J6-TEST PTS.
J7-LEDS
J8-KNOB

Figure 17-5
NPB-4000/C Main PCB Schematic (Sheet 1 of 3)

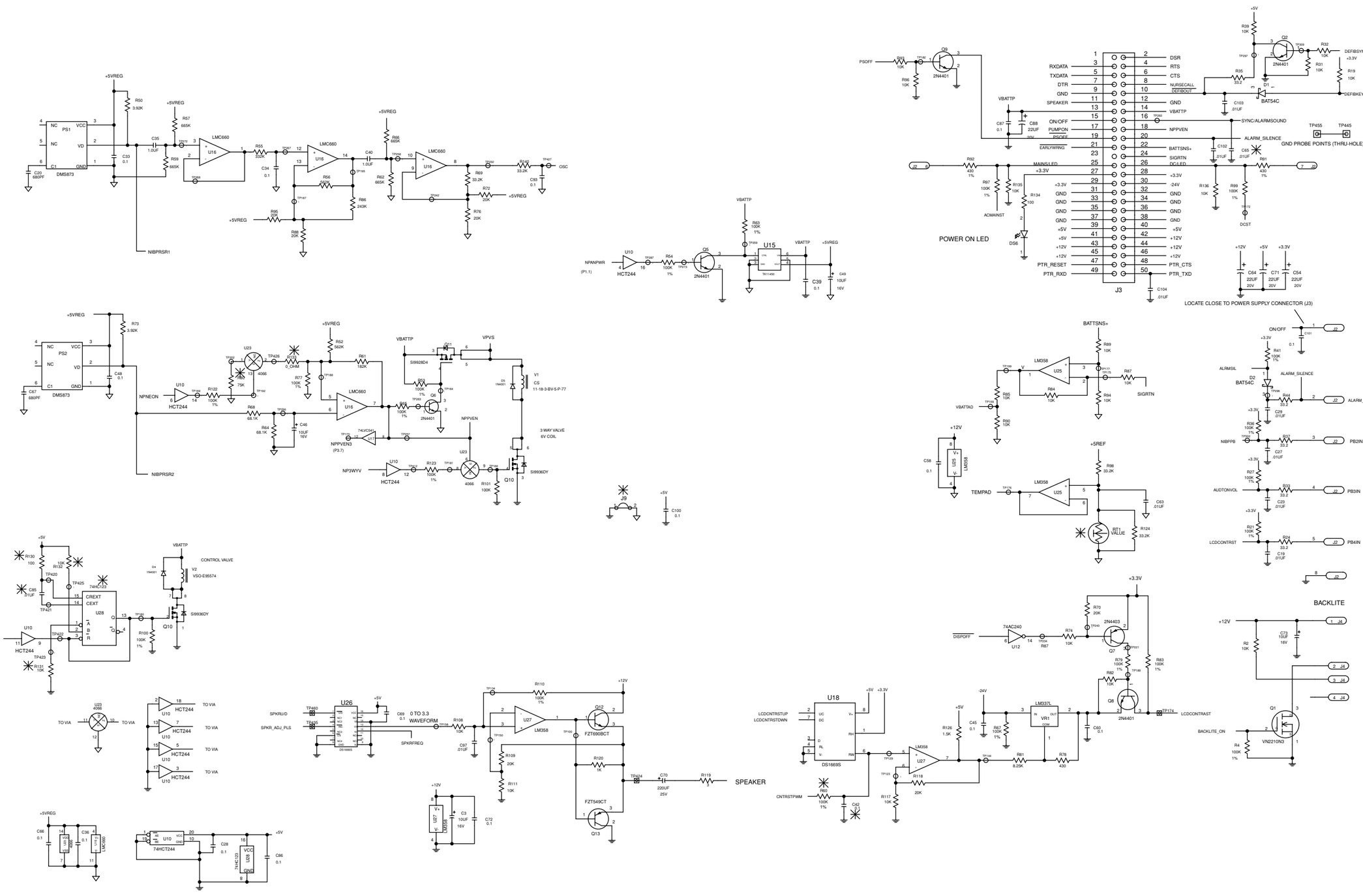

Figure 17-6
NPB-4000/C Main PCB Schematic (Sheet 2 of 3)

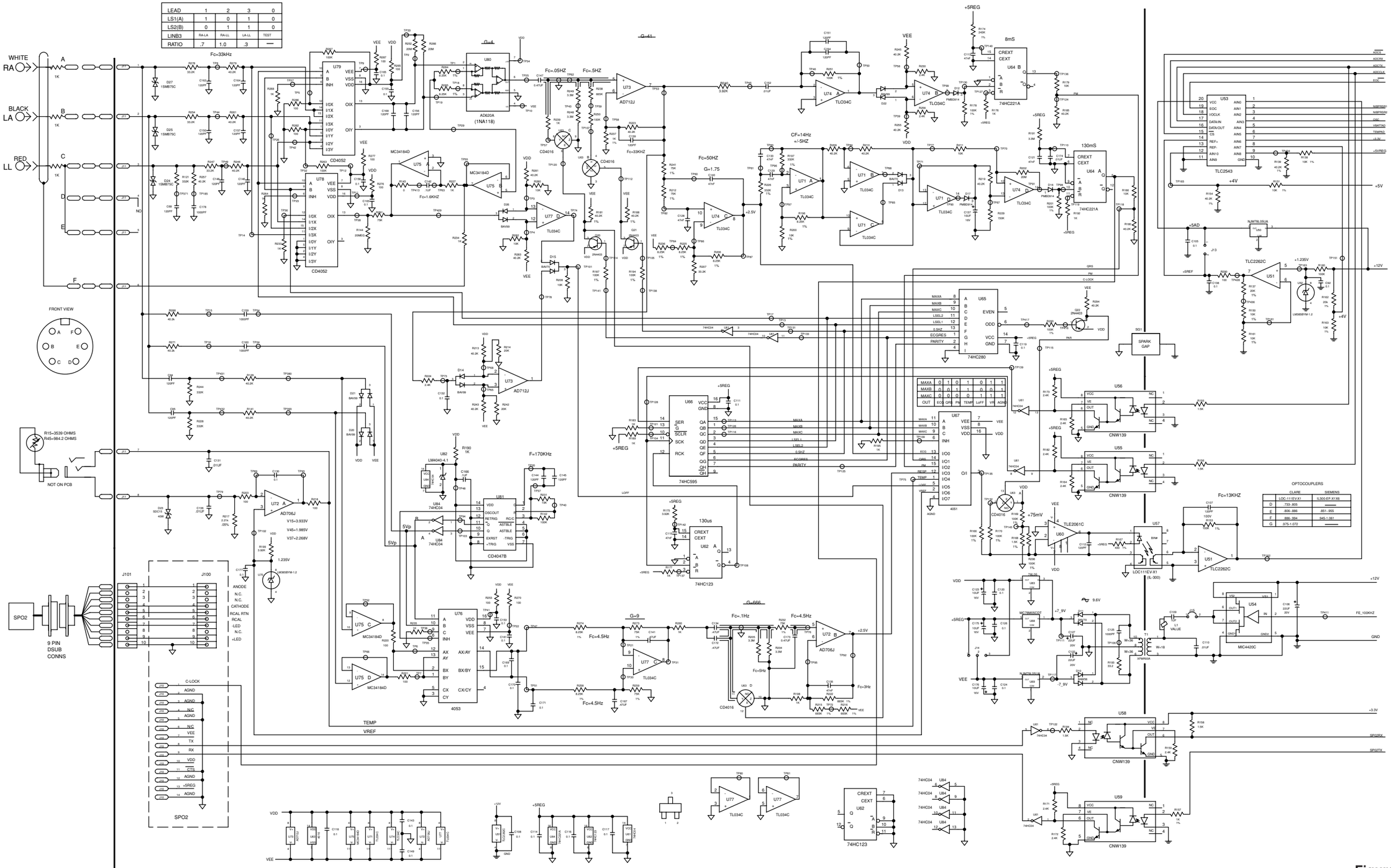

Figure 17-7
NPB-4000/C Main PCB Schematic (Sheet 3 of 3)

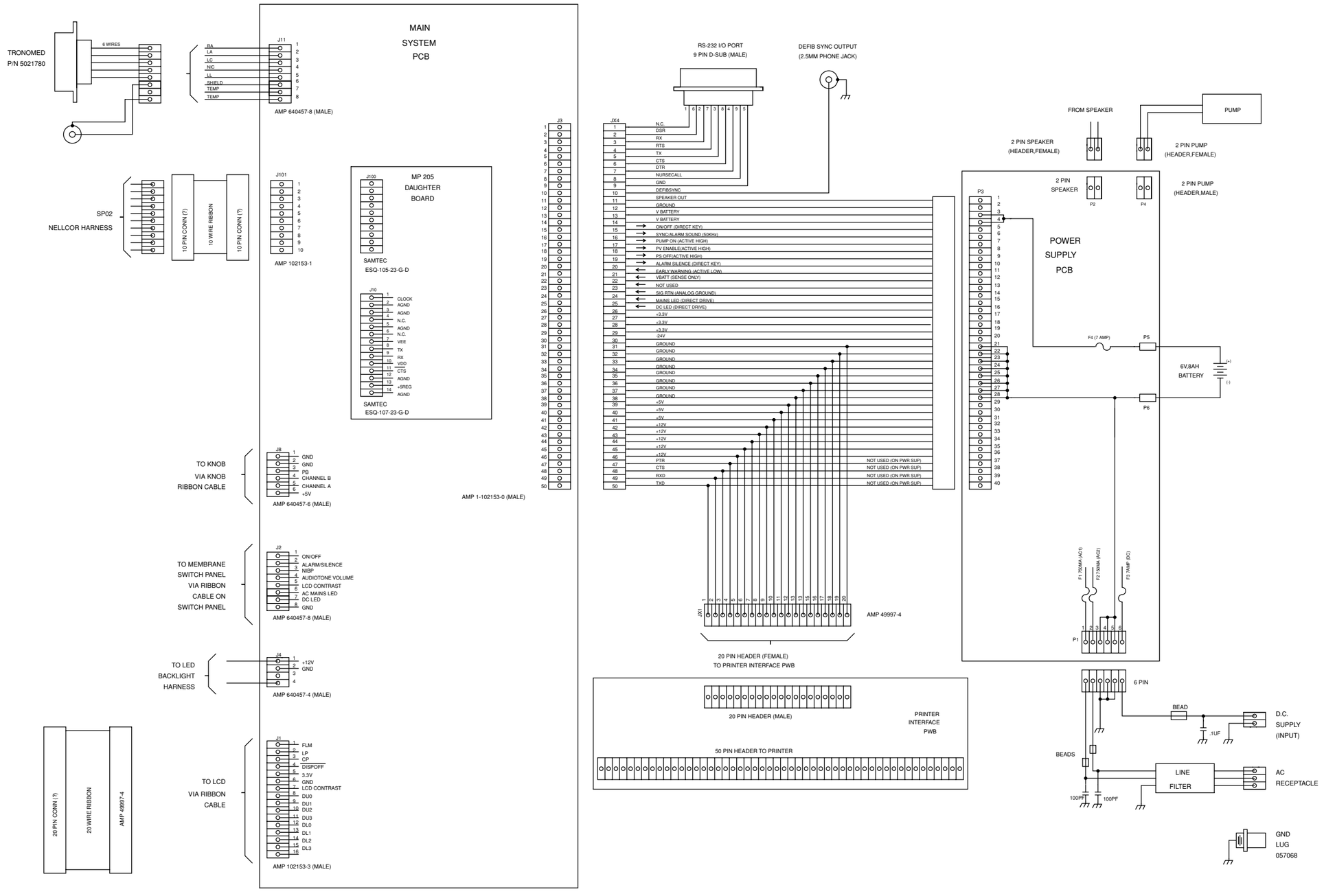

Figure 17-8
NPB-4000/C Interconnect Diagram

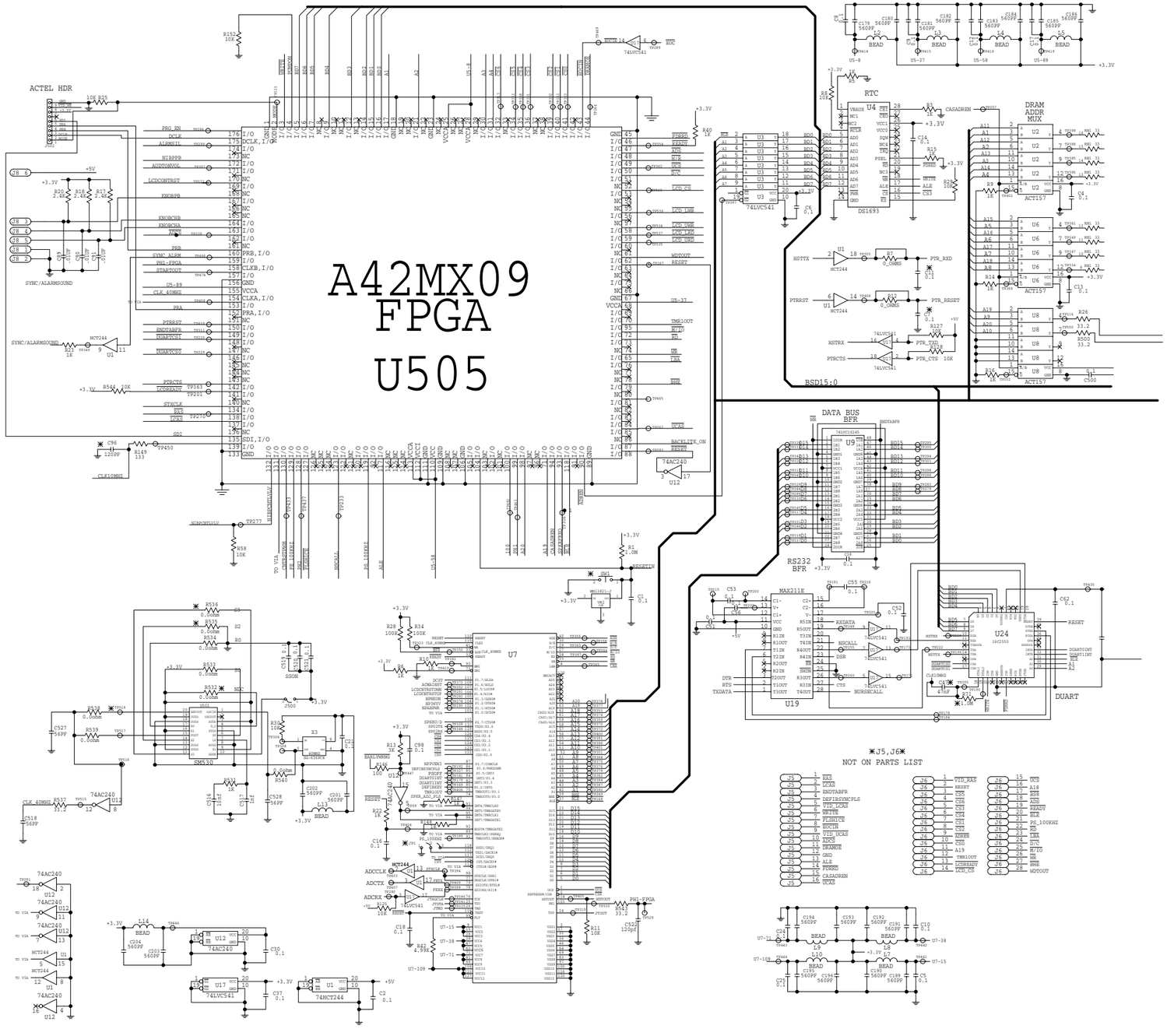

Figure 17-9
NPB-4000/C Color Motherboard Schematic